TPV

TPV COMPONENT SPECIFICATION

TPV PART NO.	PART DESCRIPTION	SUPPLIER	SUPPLIER TYPE
56G562-96	IC	GENESIS	GM2621-LF-AA
			PQFP-128
APPROVAL SHEET NO.	**QUANTITY**	**SUPPLIER CODE**	**SUPPLIER PLANT**
A050414		3000	台灣

CUSTOMS DUTY PARTS	☑YES ☐NO	CLASSIFY CODE	LE56F
SAFETY PARTS	☐YES ☑NO	SAFETY CONTROLLED MARKING	☐YES ☑NO
CERTIFICATE FOR CHINA COMPULSORY PRODUCT CERTIFICATION (CCC/CQC)			☐YES ☑NO

VERSION	B	RELEASED DATE	05/15'05	☑1st source ☐ 2nd source

NOTE:

機種：HP L1906

- RoHS 料件。
- 来料外箱 BARCODE 下方需加盖 TPV 要求之标准“RoHS”印章。
- 根据 SONY 技术标准 SS-00259 规定：所有来料(使用的原材料及辅助材料)必须符合 SS-00259 要求。
- 来料外箱及最小包装均要求标示“GP”字样。

規格書第 1-52 頁，包裝資料第 53 頁，測試報告第 0 頁，ROHS 資料第 54-60 頁，SONY 資料第 61-64 頁

注意：

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2. 零件規格的變更必須詳細記錄到版本變更履歷中，同時必須提供舊料切換控制、版本控制的方式。
3. 供应商应建立体系对其次级供应商进行管理。

NOTICE:

1. Any contents changed of component, especially material, process, die, plant, mark, equipment of key process, halftone, design, specification etc affect component electrical characteristic and reliability and working characteristic changed of production, the supplier should be inform TPV RD the changed information with TPV ECR form. Only TPV RD approval the ECR, supplier cans instruction the changed.
2. Component spec must be minute detail changed in version record, and provide old version production changed mode, version control mode.
3. The vendor need build a system to manage sub-tier.

SIGNATURE

COMPONENT ENGINEER	詹傳祥 5/15	ELECTRONIC PROJECT ENGINEER	楊明哲 5/18'2005
SAFETY ENGINEER	α	MECHANICAL PROJECT ENGINEER	
EMC ENGINEER	α	CHECKED BY	
APPROVER BY	Chuckcly 5/18/05'		

TPV COMPONENT SPEC VERSION RECORD

TPV PART NO.	56G562-96	**SUPPLIER**	GENESIS

VER	MINUTE OF CHANGES	CHECKER	RELEASE DATE
B	1.限量承認改爲正式承認	詹傳祥	5/18

gm5621 Family

PRELIMINARY Datasheet

Ordering Information

Part Number	Output Resolution	Package
gm5621-AA	SXGA	128-pin PQFP
gm5611-AA	XGA	
gm2621-AA	SXGA	
gm2611-AA	XGA	
gm5621-LF-AA	SXGA	128-pin PQFP Lead Free
gm5611-LF-AA	XGA	
gm2621-LF-AA	SXGA	
gm2611-LF-AA	XGA	

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P/N C5621-DAT-01E

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Revision History

Revision	Date	Description
C5621-DAT-01A	May 27, 2004	Initial Release
C5621-DAT-01B	July 14, 2004	- Updated pin-compatible family table in Overview - Updated pin list and diagram: changed pin names for pins 7-16, 31-40, and 63 - Updated pin descriptions in Table 7 for SPI_DI and SPI_DO - Updated Ordering Information
C5621-DAT-01C	September 7, 2004	- Updated Functional Description: - TCLK description - Replaced "Internal Oscillator Output at TCLK Pin" figure - Updated Reset pulse duration data in "Power-On Reset Specification" table - Changed AVDD 3.3 Glitch-Induced Reset Specifications to 150ns - Updated Bootstrap Configuration Pins section - Updated Electrical Specifications: - DC Characteristics: Thermal Resistance, Soldering Temperature, Vapor Phase Soldering, Power Consumption, Supply Current (including Notes) - Added "LVDS Transmitter Switching Characteristics" diagram - Added tables for LVDS Even and Odd Channels 0 to 3(1) - Updated Ordering Information: - Added gm5611 and gm2611 - Added HOST_SDA and HOST_SCL pin names to pins 66 and 67 - Added lead-free solder reflow profile diagram - Added table to title page that includes gm5621 Family derivative products (gm2621, gm5611, gm2611)
C5621-DAT-01D	December 6, 2004	- Updated Functional Description: - Removed section "Using an External Clock Oscillator" - Minor changes to Clock Generation and Clock Domains - Changes in GPIO section - Changes to note in Bootstrap Configuration - Changed pin 105 to GPO_6; updated description
C5621-DAT-01E	December 22, 2004	- Added section on Instant Auto - Moved Ordering Information to front cover - Added Lead-Free temperatures to Table 18, "Absolute Maximum Ratings"

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1 Overview

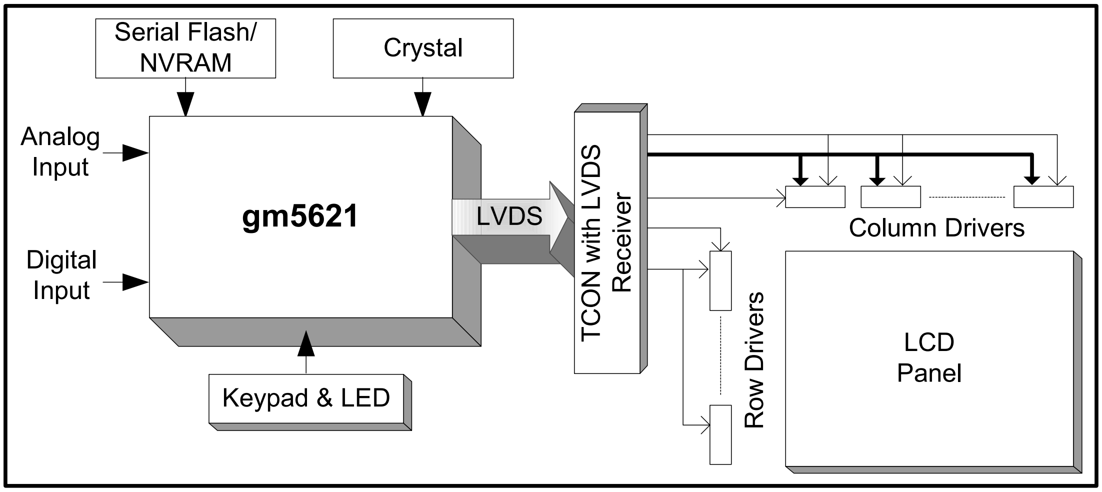
The gm5621 is an all-in-one dual input LCD monitor controller supporting resolutions up to SXGA that is available in a very low pin count package. The gm5621 leverages Genesis patented advanced image-processing technology as well as a proven integrated ADC/PLL and an Ultra-Reliable DVI™ compliant digital receiver to deliver a high-quality solution for mainstream analog and dual input monitors. gm5621 includes an on-chip, industry standard, dual channel LVDS transmitter for direct interfacing of commercially available LVDS LCD panel modules. In addition, gm5621 includes an integrated X86 OCM with SPI compatible interface, a multicolor proportional font OSD engine, a programmable coefficient scaling engine, dual channel Schmitt and Reset circuitry. Along with the high quality and reliability, gm5621 also provides a very low cost system design because of the reduction in the number of system components used and reduction in the board size due to a smaller package.

The gm5621 is part of the Genesis gm56xx family of products, which offers pin compatibility across the RSDS part, gm5626, and all of their derivative products. The pin compatible parts available in the gm56xx family are listed below:

Device	High-Quality ADC	Ultra-Reliable DVI™ Rx	HDCP Content Protection	LVDS Tx	RSDS Tx	Output Resolution	Package
gm5621	√	√		√		SXGA	128-QFP
gm5626	√	√		√	√	SXGA	128-QFP
gm5626H	√	√	√	√	√	SXGA	128-QFP
gm2621	√			√		SXGA	128-QFP
gm2626	√			√	√	SXGA	128-QFP
gm5611	√	√		√		XGA	128-QFP
gm2611	√			√		XGA	128-QFP

1.1 System Design Example

Figure 1: gm5621 System Design Example



1.2 Features

INTELLIGENT IMAGE PROCESSING™

- Programmable coefficients for user sharpness control
- Real Recovery™ function provides full color recovery image for refresh rates higher than those supported by the LCD panel

ANALOG RGB INPUT

- Supports up to SXGA 75Hz / UXGA 60Hz
- Composite-sync and Sync-on-Green (SOG) support
- Input format detection and auto-alignment
- Phase clock and image positioning

ON-CHIP MICROCONTROLLER

- High-performance 16-bit X86 MCU with on-chip RAM and ROM
- Unified memory architecture simplifies chip programming
- 7 general-purpose inputs-outputs (GPIO)
- Additional 5 general-purpose outputs (GPO), Of which 2 can be configured as PWMs
- UART link for ISP and factory setting purpose
- Two DDC2Bi with DMA buffer to internal RAM
- Slow clock mode for 50mW sleep mode power consumption
- Host I2C support for firmware debugging

HIGHLY INTEGRATED SYSTEM-ON-A-CHIP

- 50mW power saving mode
- 5-Volt tolerant inputs
- Two Layer PCB support
- On-chip reset circuit to eliminate external reset IC
- Integrated Schmitt trigger for HSYNC and VSYNC
- General purpose low bandwidth ADC

ULTRA-RELIABLE DVI™ INPUT

- Operating speed 165 MHz (up to UXGA 60Hz)
- Direct connect to all DVI-compliant digital transmitters
- High-bandwidth Digital Content Protection (HDCP)

ON-CHIP OSD CONTROLLER

- On-chip RAM for high-quality programmable menus
- 1, 2 and 4-bit per pixel character cells
- Horizontal and vertical stretch of OSD menus
- Blinking, transparency and blending
- Supports two independent OSD menu rectangles
- Proportional fonts

LVDS TRANSMITTERS

- Double pixel up to SXGA 75Hz output
- Support for 8 or 6-bit panels (with high-quality dithering)
- Pin swap, odd / even swap and red / blue group swap of RGB outputs for flexibility in board layout
- Programmable signal amplitude

2 Pin Diagrams: gm5621, gm5611, gm2621, gm2611

These devices are packaged in a 128-pin Plastic Quad Flat Pack (PQFP).

Figure 2: gm5621 Pinout

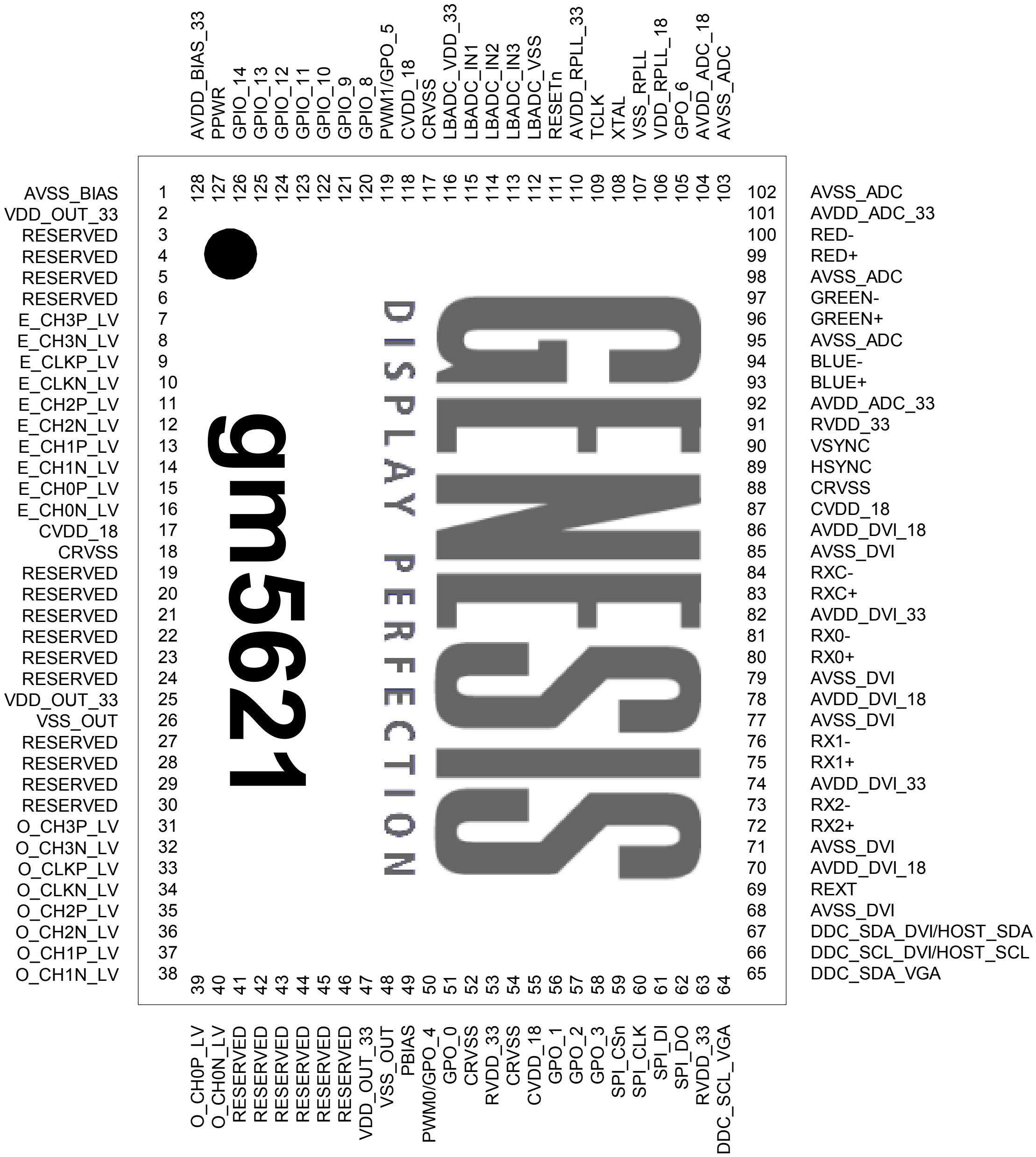


Figure 3: gm5611 Pinout

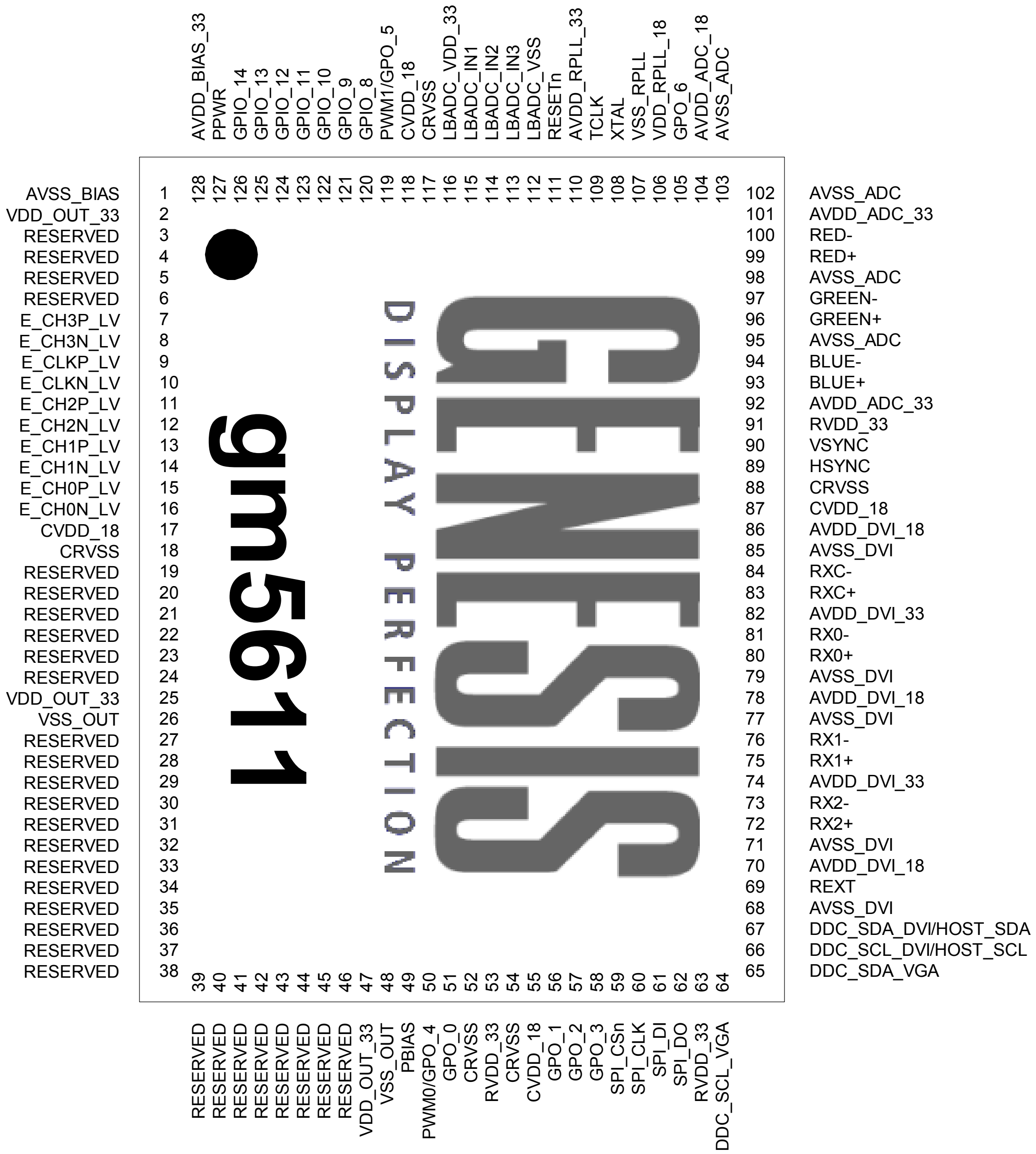


Figure 4: gm2621 Pinout

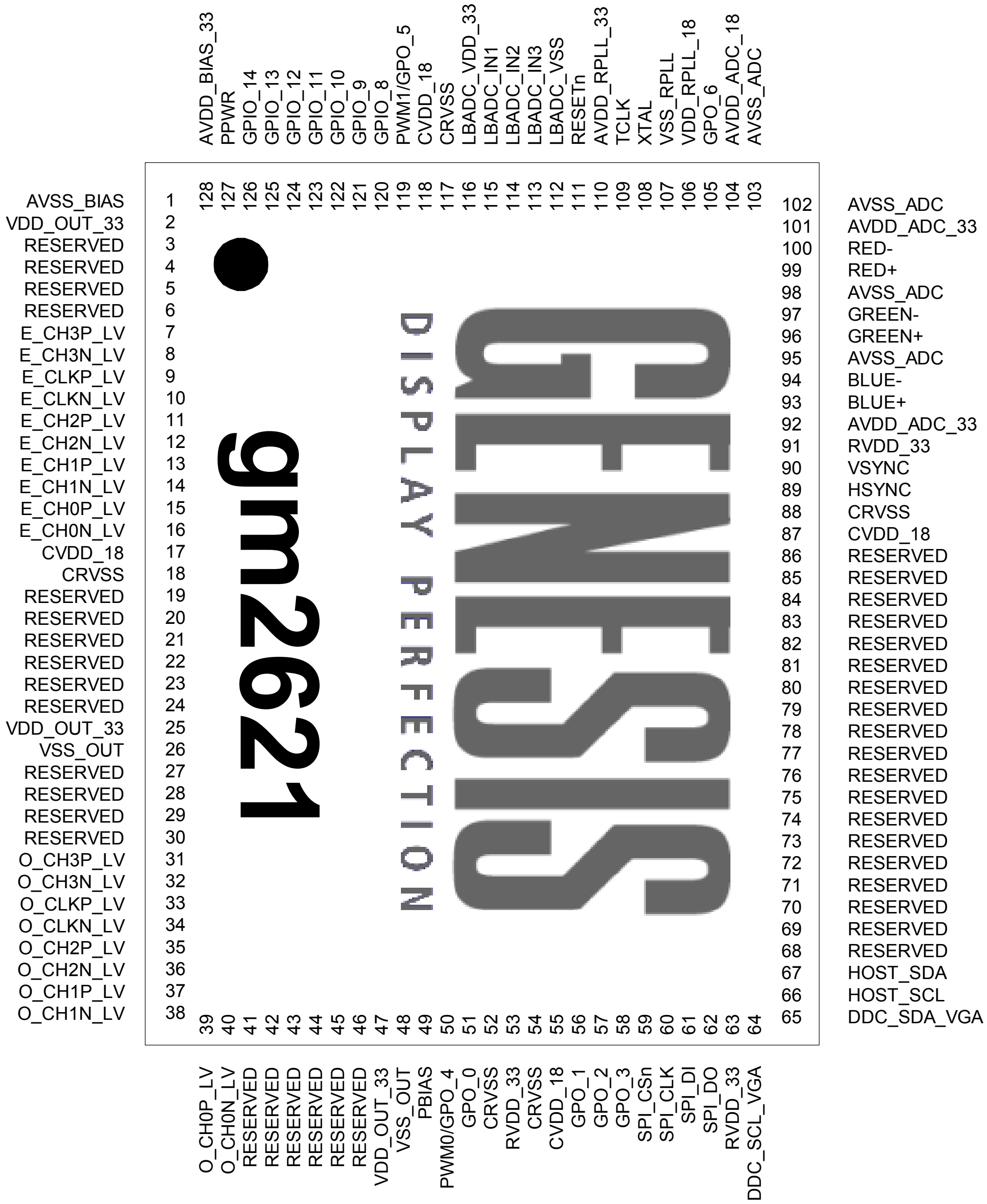
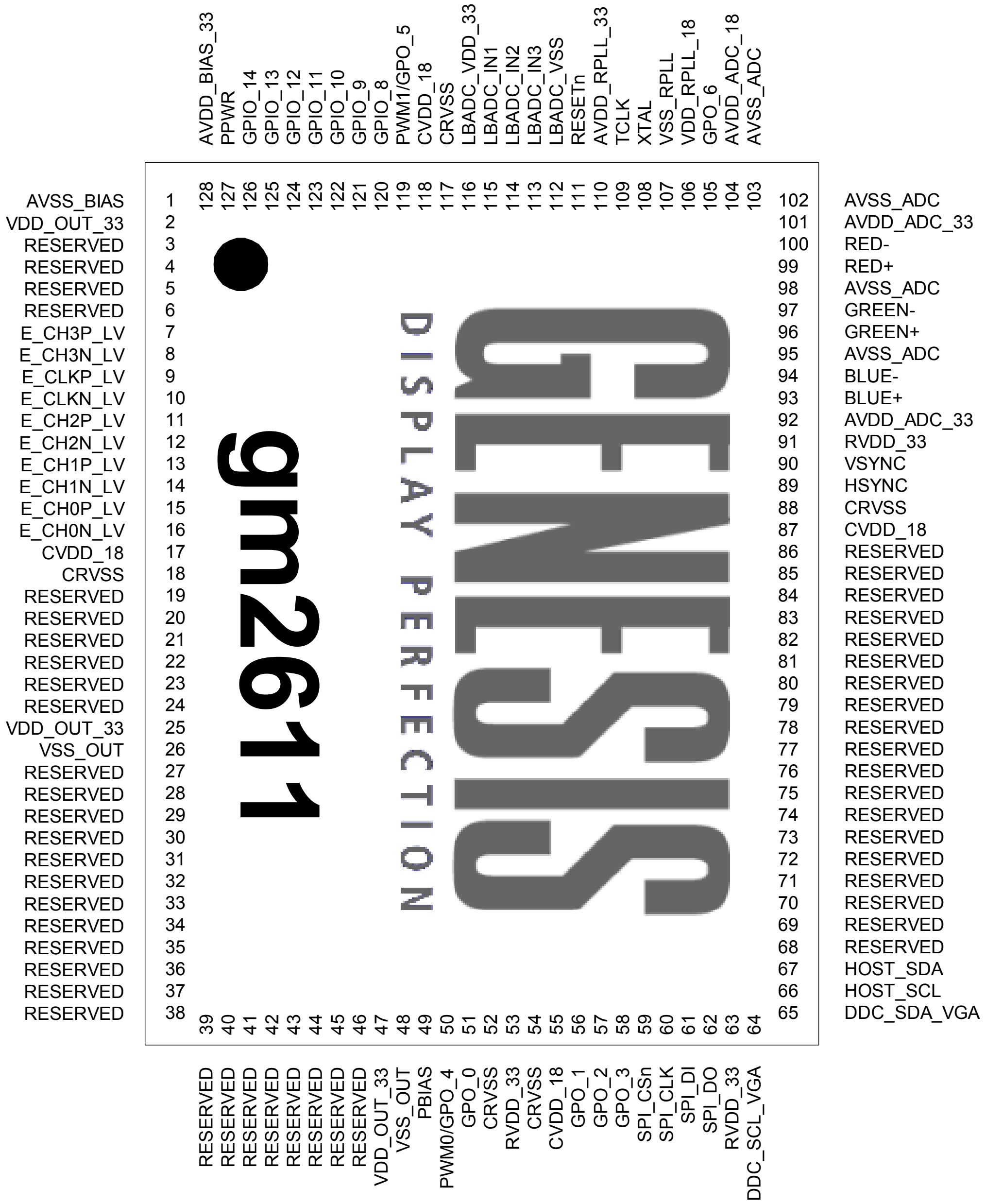


Figure 5: gm2611 Pinout



3 Pin List: gm5621/gm5611/gm2621/gm2611

I/O Legend: A = Analog, **I** = Input, **O** = Output, **P** = Power, **G**= Ground

Table 1: LVDS Panel Interface

Pin Name	No	I/O	Description
AVSS_BIAS	1	AG	Analog ground for LVDS PLL and Bandgap
VDD_OUT_33	2	P	Digital 3.3V supply for LVDS output
RESERVED	3	AO	Reserved; Do not connect
RESERVED	4	AO	Reserved; Do not connect
RESERVED	5	AO	Reserved; Do not connect
RESERVED	6	AO	Reserved; Do not connect
E_CH3P_LV	7	AO	LVDS even channel 3 positive
E_CH3N_LV	8	AO	LVDS even channel 3 negative
E_CLKP_LV	9	AO	LVDS even channel clock positive
E_CLKN_LV	10	AO	LVDS even channel clock negative
E_CH2P_LV	11	AO	LVDS even channel 2 positive
E_CH2N_LV	12	AO	LVDS even channel 2 negative
E_CH1P_LV	13	AO	LVDS even channel 1 positive
E_CH1N_LV	14	AO	LVDS even channel 1 negative
E_CH0P_LV	15	AO	LVDS even channel 0 positive
E_CH0N_LV	16	AO	LVDS even channel 0 negative
RESERVED	19	AO	Reserved; Do not connect
RESERVED	20	AO	Reserved; Do not connect
RESERVED	21	AO	Reserved; Do not connect
RESERVED	22	AO	Reserved; Do not connect
RESERVED	23	AO	Reserved; Do not connect
RESERVED	24	AO	Reserved; Do not connect
VDD_OUT_33	25	P	Digital 3.3V supply for LVDS output
VSS_OUT	26	G	Digital ground for LVDS output
RESERVED	27	AO	Reserved; Do not connect
RESERVED	28	AO	Reserved; Do not connect
RESERVED	29	AO	Reserved; Do not connect
RESERVED	30	AO	Reserved; Do not connect
O_CH3P_LV	31	AO	LVDS odd channel 3 positive. Reserved for gm5611 and gm2611.
O_CH3N_LV	32	AO	LVDS odd channel 3 negative. Reserved for gm5611 and gm2611.
O_CLKP_LV	33	AO	LVDS odd channel clock positive. Reserved for gm5611 and gm2611.
O_CLKN_LV	34	AO	LVDS odd channel clock negative. Reserved for gm5611 and gm2611.
O_CH2P_LV	35	AO	LVDS odd channel 2 positive. Reserved for gm5611 and gm2611.
O_CH2N_LV	36	AO	LVDS odd channel 2 negative. Reserved for gm5611 and gm2611.
O_CH1P_LV	37	AO	LVDS odd channel 1 positive. Reserved for gm5611 and gm2611.
O_CH1N_LV	38	AO	LVDS odd channel 1 negative. Reserved for gm5611 and gm2611.
O_CH0P_LV	39	AO	LVDS odd channel 0 positive. Reserved for gm5611 and gm2611.
O_CH0N_LV	40	AO	LVDS odd channel 0 negative. Reserved for gm5611 and gm2611.
RESERVED	41	AO	Reserved; Do not connect
RESERVED	42	AO	Reserved; Do not connect
RESERVED	43	AO	Reserved; Do not connect
RESERVED	44	AO	Reserved; Do not connect
RESERVED	45	AO	Reserved; Do not connect
RESERVED	46	AO	Reserved; Do not connect
VDD_OUT_33	47	P	Digital 3.3V supply for LVDS output
VSS_OUT	48	G	Digital ground for LVDS output
AVDD_BIAS_33	128	AP	Analog 3.3V supply for LVDS PLL and Bandgap
PBIAS	49	O	Panel backlight enable
PPWR	127	O	Panel power enable

Table 2: VGA Analog Input Port

Pin Name	No	I/O	Description
HSYNC	89	I	ADC input horizontal sync or composite sync input. [Input, programmable Schmitt Trigger, 5V-tolerant]
VSYNC	90	I	ADC input vertical sync. [Input, programmable Schmitt Trigger, 5V-tolerant]
AVDD_ADC_33	92	AP	Analog power (3.3V) for ADC.
BLUE+	93	AI	Positive analog input for Blue channel.
BLUE-	94	AI	Negative analog input for Blue channel.
AVSS_ADC	95	AG	Analog ground for ADC.
GREEN+	96	AI	Positive analog input for Green channel and SOG input.
GREEN-	97	AI	Negative analog input for Green channel.
AVSS_ADC	98	AG	Analog ground for ADC.
RED+	99	AI	Positive analog input for Red channel.
RED-	100	AI	Negative analog input for Red channel.
AVDD_ADC_33	101	AP	Analog power (3.3V) for ADC. Must be bypassed with capacitor to AVSS_ADC pin.
AVSS_ADC	102	AG	Analog ground for ADC.
AVSS_ADC	103	AG	Analog ground for ADC.
AVDD_ADC_18	104	AP	Analog power (1.8V) for ADC. Must be bypassed with capacitor to AVSS_ADC pin.

Table 3: DVI Receiver

Pin Name	No	I/O	Description
AVSS_DVI	68	AG	Analog GND for DVI input. Reserved for gm2621 and gm2611; Do not connect.
REXT	69	AI	External reference resistor. A 1%, 250Ω resistor should be connected from this pin to pin 74. Reserved for gm2621 and gm2611; Do not connect.
AVDD_DVI_18	70	AP	Analog VDD (1.8V) for DVI input. Must be bypassed with external capacitor(s) to AVSS_DVI. Reserved for gm2621 and gm2611; Do not connect.
AVSS_DVI	71	AG	Analog GND for DVI input. Reserved for gm2621 and gm2611; Do not connect.
RX2+	72	AI	DVI input channel 2 positive. Reserved for gm2621 and gm2611; Do not connect.
RX2-	73	AI	DVI input channel 2 negative. Reserved for gm2621 and gm2611; Do not connect.
AVDD_DVI_33	74	AP	Analog VDD (3.3V) for DVI input. Reserved for gm2621 and gm2611; Do not connect.
RX1+	75	AI	DVI input channel 1 positive. Reserved for gm2621 and gm2611; Do not connect.
RX1-	76	AI	DVI input channel 1 negative. Reserved for gm2621 and gm2611; Do not connect.
AVSS_DVI	77	AG	Analog GND for DVI input. Reserved for gm2621 and gm2611; Do not connect.
AVDD_DVI_18	78	AP	Analog VDD (1.8V) for DVI input. Must be bypassed with external capacitor(s) to AVSS_DVI. Reserved for gm2621 and gm2611; Do not connect.
AVSS_DVI	79	AG	Analog GND for DVI input. Reserved for gm2621 and gm2611; Do not connect.
RX0+	80	AI	DVI input channel 0 positive. Reserved for gm2621 and gm2611; Do not connect.
RX0-	81	AI	DVI input channel 0 negative. Reserved for gm2621 and gm2611; Do not connect.
AVDD_DVI_33	82	AP	Analog VDD (3.3V) for DVI input. Reserved for gm2621 and gm2611; Do not connect.
RXC+	83	AI	DVI clock input positive. Reserved for gm2621 and gm2611; Do not connect.
RXC-	84	AI	DVI clock input negative. Reserved for gm2621 and gm2611; Do not connect.
AVSS_DVI	85	AG	Analog GND for DVI input. Reserved for gm2621 and gm2611; Do not connect.
AVDD_DVI_18	86	AP	Analog VDD (1.8V) for DVI input. Must be bypassed with external capacitor(s) to AVSS_DVI. Reserved for gm2621 and gm2611; Do not connect.

Table 4: CLOCKS

Pin Name	No	I/O	Description
VDD_RPLL_18	106	P	Digital 1.8V power for PLL.
VSS_RPLL	107	G	Ground for PLL.
XTAL	108	AO	Connect to 14.3MHz crystal. Should be bypassed with capacitor to AVDD_RPLL_33.
TCLK	109	AI	Connect to 14.3MHz crystal. Should be bypassed with capacitor to AVDD_RPLL_33.
AVDD_RPLL_33	110	AP	Analog power (3.3V) for PLL.

Table 5: Digital Power and Ground

Pin Name	No	I/O	Description
RVDD_33	53 63 91	P	Digital output VDD. Connect to digital 3.3V.
CVDD_18	17 55 87 118	P	Core VDD. Connect to digital 1.8V.
CRVSS	18 52 54 88 117	G	Chip digital ground.

Table 6: System Interface

Pin Name	No	I/O	Description
DDC_SCL_VGA	64	I	DDC2Bi clock for Analog Port
DDC_SDA_VGA	65	IO	DDC2Bi data for Analog Port, internal pullup of 10K ohms.
DDC_SCL_DVI/ HOST_SCL	66	I	DDC2Bi clock for DVI Port or host 2-wire clock signal for debugging.
DDC_SDA_DVI/ HOST_SDA	67	IO	DDC2Bi data for DVI Port or host 2-wire data signal for debugging, internal pullup of 10K ohms.
GPO_0	51	IO	General-purpose output GPO_0. Also used for bootstrap control.
GPO_1	56	IO	General-purpose output GPO_1. Also used for bootstrap control.
GPO_2	57	IO	General-purpose input/output GPO_2. Also used for bootstrap control.
GPO_3	58	IO	General-purpose output GPO_3. Also used for bootstrap control.
PWM0 / GPO_4	50	IO	PWM0 output or optional general-purpose output GPO_4. Also used for bootstrap control.
GPO_6	105	O	General-purpose output GPO_6. Output drive limited to 1.8V only.
PWM1 / GPO_5	119	IO	PWM1 output or optional general-purpose output GPO_5. Also used for bootstrap control.
RESETn	111	AIO	Bypass with 0.01uF capacitor to GND.
GPIO_8	120	IO	General-purpose input/output 8
GPIO_9	121	IO	General-purpose input/output 9
GPIO_10	122	IO	General-purpose input/output 10
GPIO_11	123	IO	General-purpose input/output 11
GPIO_12	124	IO	General-purpose input/output 12
GPIO_13	125	IO	General-purpose input/output 13
GPIO_14	126	IO	General-purpose input/output 14

Note: In gm2621 and gm2611, pins 66 and 67 are available for host 2-wire purposes only.

Table 7: General-Purpose LBADC

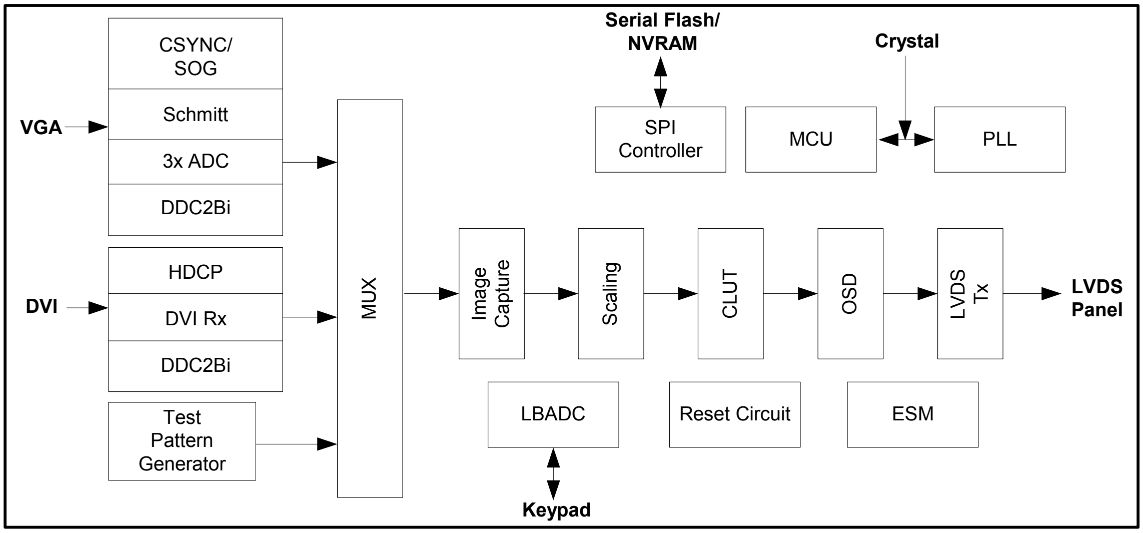
Pin Name	No	I/O	Description
LBADC_VSS	112	G	Ground for general-purpose LBADC.
LBADC_IN3	113	AI	General-purpose LBADC input 3.
LBADC_IN2	114	AI	General-purpose LBADC input 2.
LBADC_IN1	115	AI	General-purpose LBADC input 1.
LBADC_VDD_33	116	P	3.3V supply for general-purpose LBADC. Connect to the same power rail as RVDD_33.

Table 8: SPI ROM

Pin Name	No	I/O	Description
SPI_CSn	59	IO	SPI ROM chip select. Also used for bootstrap control.
SPI_CLK	60	IO	SPI ROM Clock output.
SPI_DI	61	IO	SPI ROM Data input. Connect this pin to the data output of Serial FLASH.
SPI_DO	62	IO	SPI ROM Data output. Connect this pin to the data input of Serial FLASH.

4 Functional Description

Figure 6: Functional Block Diagram



4.1 Clock Generation

The following input sources are accepted:

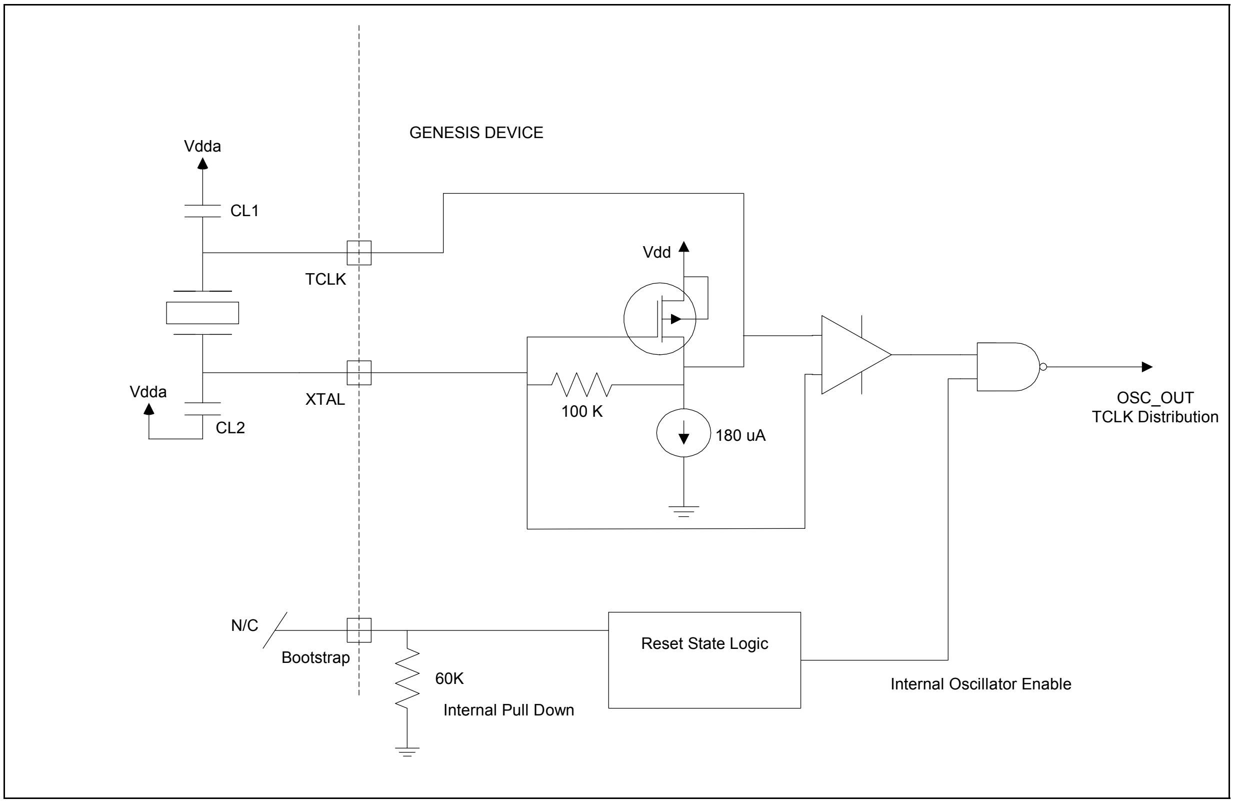
1. Crystal Input Clock (TCLK and XTAL). This is the input pair to an internal crystal oscillator and corresponding logic. Alternatively, a single ended TTL/CMOS clock input can be driven into the TCLK pin (leave XTAL as n/c in this case). However, this is not recommended from the system cost saving perspective.
2. DVI Differential Input Clock (RC+ and RC-).
3. Two I2C slave SCLs for DDC2Bi (one is also for I2C-to-JTAG bridge).

4.1.1 Clock Generation Using Internal Oscillator with External Crystal

The recommended option for providing a clock reference is to use the internal oscillator with an external crystal of 14.318MHz. The oscillator circuit is designed to provide a very low jitter and very low harmonic clock to the internal circuitry of the chip. An Automatic Gain Control (AGC) is used to insure startup and operation over a wide range of conditions. The oscillator circuit also minimizes the overdrive of the crystal, which reduces the aging of the crystal.

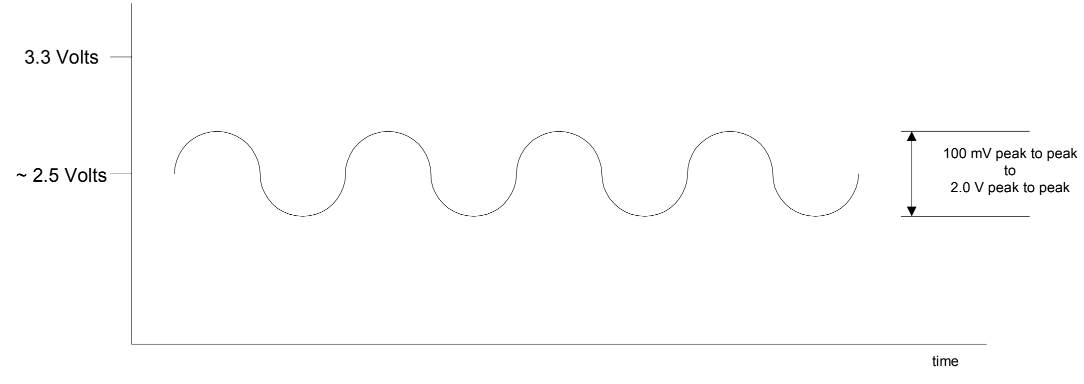
When the internal oscillator is enabled, a crystal resonator is connected between TCLK and the XTAL with the appropriately sized loading capacitors C_{L1} and C_{L2}. The size of C_{L1} and C_{L2} are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the Genesis device and the printed circuit board traces. The loading capacitors are terminated to the analog VDD power supply. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to ground.

Figure 7: Clock Generation Using Internal Oscillator with External Crystal



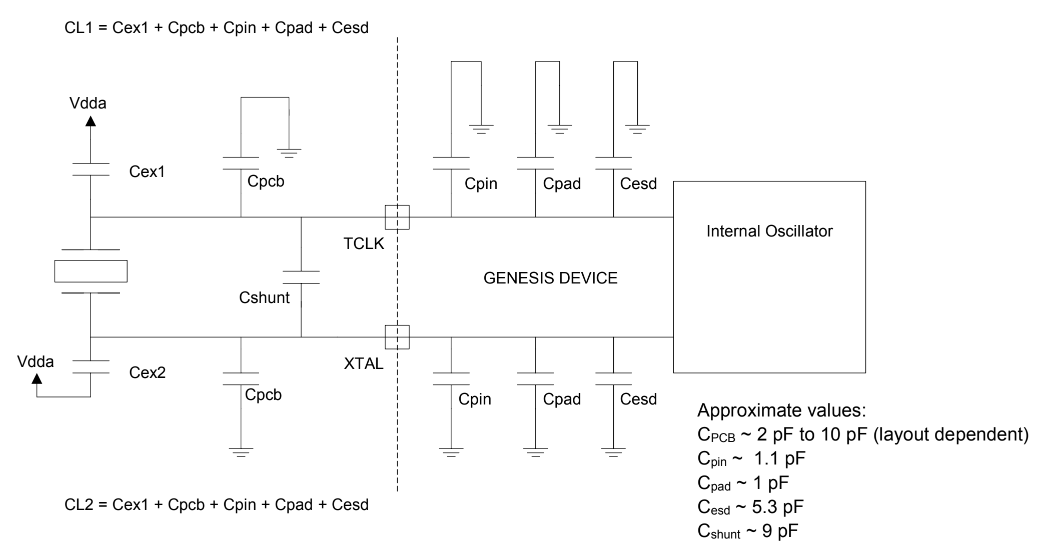
The TCLK oscillator uses a Pierce Oscillator circuit. The output of the oscillator circuit, measured at the TCLK pin, is an approximate sine wave with a bias of about 2.5 volts above ground (see the figure below, “Internal Oscillator Output at TCLK Pin”). The peak-to-peak voltage of the output (measured at TCLK Pin) can range from 100 mV to 2.0 V. This range is provided as a reference; the actual peak-to-peak voltage range and bias on the TCLK pin may vary depending on the specific characteristics of the crystal, the PCB traces and load of the capacitors variations. The maximum voltage level of the peak-to-peak swing cannot exceed 3.6 V (see “Absolute Maximum Ratings” Table). The internal oscillator requires a minimum signal level greater than 100-mV peak-to-peak to function. If the peak-to-peak range falls below 100 mV, the internal oscillator will not work. The output of the oscillator is connected to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50-mV peak to peak to function correctly. The output of the comparator is buffered and then distributed to the internal circuits.

Figure 8: Internal Oscillator Output at TCLK Pin



One of the design parameters that must be given some consideration is the value of the loading capacitors used with the crystal. The loading capacitance (C_{load}) on the crystal is the combination of C_{L1} and C_{L2} and is calculated by $C_{load} = ((C_{L1} * C_{L2}) / (C_{L1} + C_{L2})) + C_{shunt}$. The shunt capacitance C_{shunt} is the effective capacitance between the XTAL and TCLK pins. On this chip, it is approximately 9 pF. C_{L1} and C_{L2} are a parallel combination of the external loading capacitors (C_{ex}), the PCB board capacitance (C_{pcb}), the pin capacitance (C_{pin}), the pad capacitance (C_{pad}), and the ESD protection capacitance (C_{esd}). The capacitances are symmetrical so that $C_{L1} = C_{L2} = C_{ex} + C_{PCB} + C_{pin} + C_{pad} + C_{ESD}$. The correct value of C_{ex} must be calculated based on the values of the load capacitances.

Figure 9: Sources of Parasitic Capacitance



Approximate values:
C_{PCB} ~ 2 pF to 10 pF (layout dependent)
C_{pin} ~ 1.1 pF
C_{pad} ~ 1 pF
C_{esd} ~ 5.3 pF
C_{shunt} ~ 9 pF

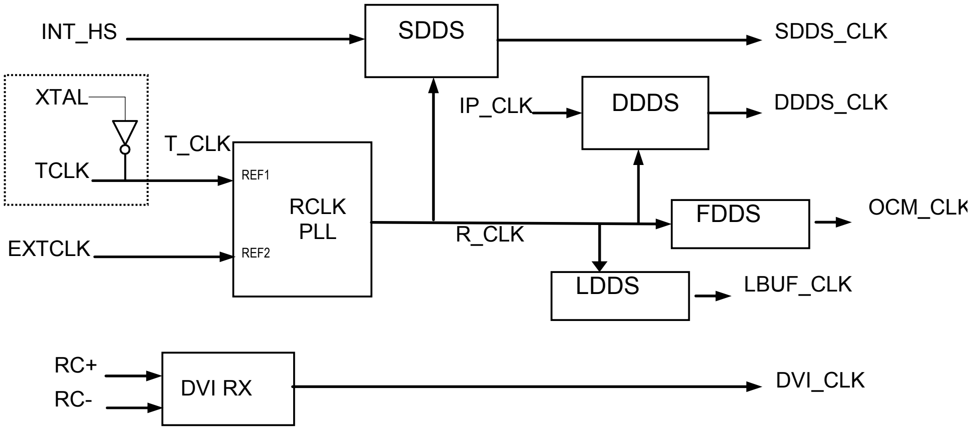
Some attention must be given to the details of the oscillator circuit when used with a crystal resonator. The PCB traces should be as short as possible. The value of C_{load} that is specified by the manufacturer should not be exceeded because of potential start up problems with the oscillator. Additionally, the crystal should be a parallel resonate-cut and the value of the equivalent series resistance must be less then 90 Ω.

4.1.2 Clock Synthesis

Additional synthesized clocks:

1. Main Timing Clock (T_CLK) is the output of the chip internal crystal oscillator. T_CLK is derived from the TCLK/XTAL pad input.
2. Reference Clock (R_CLK) synthesized by RCLK PLL using T_CLK or EXTCLK as the reference.
3. DVI Output Clock (DVI_CLK) synthesized by DVI receiver PLL using RC+/RC-as the reference.
4. Input Source Clock (SDDS_CLK) synthesized by SDDS PLL using input HS as the reference. The SDDS also uses the R_CLK to drive internal digital logic.
5. Display Clock (DDDS_CLK) synthesized by DDDS PLL using IP_CLK as the reference. The DDDS also uses the R_CLK to drive internal digital logic.
6. Fixed Frequency Clock (FCLK) synthesized by FDDS. Used as OCM_CLK domain driver.
7. ADC Output Clock (ACLK_SENSE) is a delayed A_CLK. The analog ADC performs the adjustment.
8. Expander Line Buffer Clock (LBUF_CLK). A fixed frequency clock created by LDDS (LCLK) to drive the expander line buffer at a clock rate greater than either SDDS_CLK or DDDS_CLK.

Figure 10: Internally Synthesized Clocks



4.1.3 Clock Domains

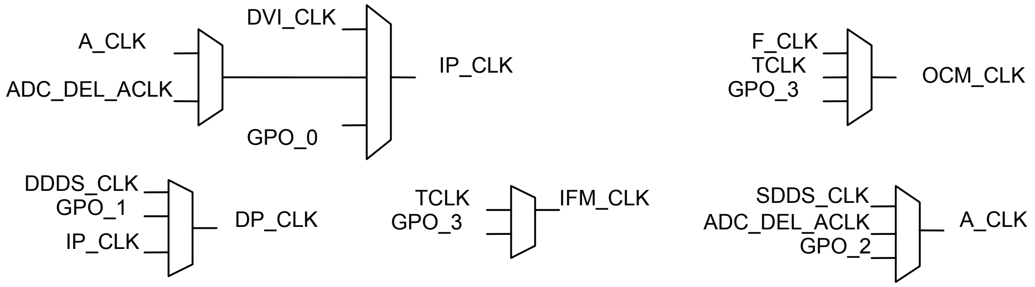
Internally, there are several clock domains.

1. Input Clock Domain (IP_CLK). Max = 165MHz
2. Input Clock Domain (T_CLK). Max = 24MHz.

3. Host Interface and On-chip Micro-controller Clock (OCM_CLK). Max = 100MHz
4. Filter and Display Pixel Clock (DP_CLK). Max = 135MHz
5. Source Timing Measurement Domain (IFM_CLK). Max = 50MHz
6. Reference Clock Domain (R_CLK output by RCLK PLL). Max = 220 MHz
7. ADC Clock Domain (A_CLK). Max = 165MHz.
8. DVI Internal Half Clock (FCREF). Max = 83 MHz (half 165 MHz).
9. Word Assembler Clock Domain (WA_CLK). Max = 413MHz.
10. Line Buffer Clock (LBUF_CLK). Max = 180Mhz

The clock selection for each domain, as shown in the figure below, is controlled using the CLOCK_CONFIG register.

Figure 11: On-Chip Clock Domains



Additional notes on clock domains:

1. The T_CLK is the output from a crystal oscillator embedded within the analog clock block. The external connection to the oscillator is via the TCLK and XTAL pads. All logic in the IC using T_CLK as an input reference source assumes T_CLK will operate at a frequency between 14MHz to 24MHz. In lieu of using a crystal oscillator, the TCLK input pad can be driven with a single ended TTL/CMOS input clock (eg. for testing of the IC); XTAL would be n/c in this case.
2. Analog ADC Clock Domain (A_CLK) is contained within the analog ADC block and the digital capture logic, immediately after the analog ADC. Source of A_CLK is programmable to be SDDS_CLK. Max of A_CLK can be set to 165 MHz.
3. The DVI internal half clock (FCREF) is generated within the Word Assembler and operated at half the pixel clock. It is used to drive the phase picker, receiver/framer, Re-synchronizer, and DVI decoder. The final stage of the DVI digital logic converts double-wide pixel data (clock with RCREF) to single-wide pixel data (clocked by IP_CLK). The DVI_dll block generates DVI_CLK such that FCREF and IP_CLK are phase separated (IP_CLK is a buffered version of DVI_CLK) to ensure no setup/hold violation during the double to single-wide pixel conversion.

4. The Word Assembler clock is internal to the DVI design. It is used at the analog/digital interface within the DVI receiver to capture high bit rate data at a rate
   F_{WA_CLK} = { (samples/symbol) x (bits per WA output clock) / (bits per WA input clock) }x $f_{PixelRate}$= 3 x 20 / 12 x $f_{PixelRate}$ = 3 x 20 / 12 x 165 MHz (max) = 413MHz.

4.2 Chip Initialization

4.2.1 Power Sequencing

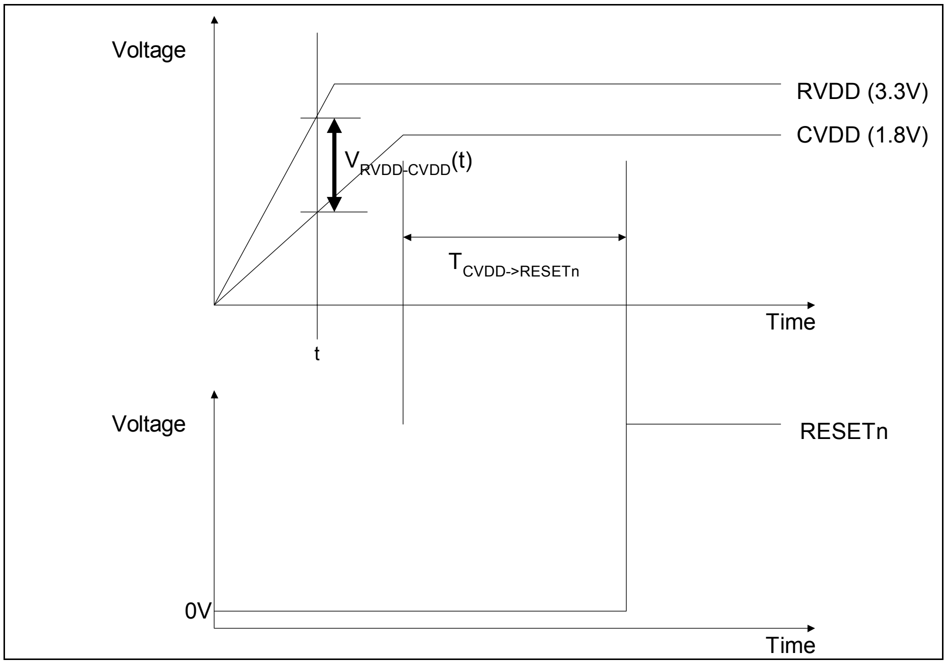
At any time during the power-up sequence, the actual voltage of the 3.3V RVDD power supply should always be equal to or higher than the actual voltage of the 1.8V CVDD power supply. In mathematical terms, V_{RVDD} >= V_{CVDD} at all times.

In addition, the system designer must ensure that the 1.8V core VDD supply must be active for at least 1ms before the rising edge of the chip RESETn signal during the chip power-up sequence. The rising edge of RESETn signal is used to latch the bootstrap configurations, so its correct timing relationship to the core VDD is critical for correct chip operation.

Table 9: Power Sequencing Requirements

Parameter	Min	Typ	Max
VRVDD-CVDD(for all t>0)	0V		
TCVDD->RESETn	150ms		

Figure 12: Correct Power Sequencing

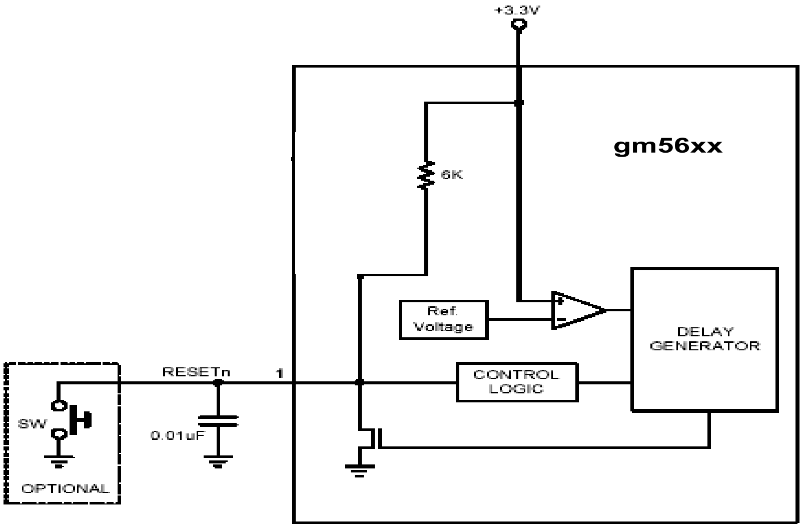


4.2.2 Hardware Reset

gm56xx devices have an integrated internal reset pulse generator, so that an external reset IC is not required.

The internal circuitry of the RESET is shown below.

Figure 13: Internal RESET Circuitry



The internal reset pulse generator performs hardware reset under the following conditions:

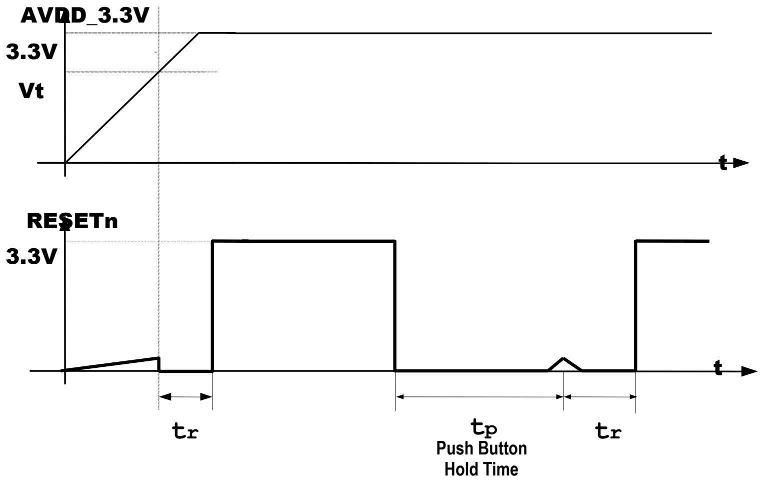
- During system power-up, after the AVDD_3.3V voltage has reached threshold Vt.
- In the event AVDD_3.3V voltage drops below threshold Vt for more than approximately 150ns.
- Manually holding the RESETn pin low for a minimum of 1ms.

The active-low reset pulse on the RESETn pin generated by the internal reset pulse generator is around 80ms (minimum) in duration. TCLK input must be applied during and after the reset. When the reset period is complete, and RESETn state becomes high, the reset sequence is as follows:

1. Reset all registers of all types to their default state (this is 00h unless otherwise specified in the Register Listing).
2. Force each clock domain into reset. This continues for 64 local clock domain cycles following the de-assertion of RESETn.
3. Operate the OCM_CLK domain at the TCLK frequency.

The following figure shows the relationship between AVDD_3.3V and RESETn during system power-up.

Figure 14: Power-up Reset Sequence Between AVDD_3.3V and RESETn Pin



NOTE: Vt is the power-up reset threshold voltage, Tr is the reset pulse duration, and Tp is the push-button hold time (the duration of holding RESETn pin low).

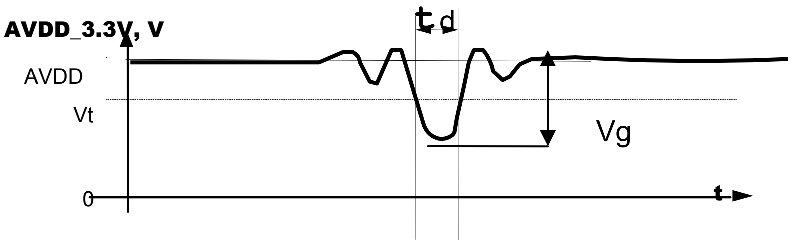
The power-on reset specifications are listed in the following table.

Table 10: Power-On Reset Specification

Description	Symbol	Min.	Typical	Max
Power-on reset threshold voltage	Vt	2.10V	2.20V	2.40V
Reset pulse duration	Tr	80ms		100ms
Push-button hold time	Tp	1ms		

There is a glitch filter in the internal reset pulse generator that ignores the AVDD_3.3V power line glitch if the glitch duration is shorter than approximately 150ns. However, if AVDD_3.3V voltage drops below the threshold Vt for more than 150ns in duration, reset will be asserted and RESETn signal will go low. The following figure illustrates the AVDD_3.3V glitch.

Figure 15: AVDD_3.3V Glitch



`td = Duration of AVDD glitch at Vt,`
`Vg = Amplitude of AVDD glitch`

Table 11: AVDD_3.3V Glitch-Induced Reset Specifications

Description	Symbol	Min.	Typical	Max
AVDD_3.3V glitch duration	Tg	150ns		
AVDD_3.3V glitch amplitude	Vg	0.9V*		1.2V*

* The AVDD_3.3V voltage must fall by more than Vg below the supply voltage (3.3V nominal) for the reset to assert (RESETn becomes low). For example, AVDD_3.3V voltage level must fall below at least 2.4V (3.3V – 0.9V) in order for reset to assert.

NOTE: The RESETn pin should be connected to ground with a 0.01uF capacitor to avoid spurious reset conditions caused by board noise.

4.2.3 Software Reset

Main blocks may be independently hardware reset by setting software reset bits in the SOFT_RESETS register.

Software Reset is performed by programming the HOST_CONTROL register bit SOFT_RESET=0. The SOFT_RESET bit will self clear to 0 upon completion of reset. A software reset

1. Resets all active registers and status registers. Pending and read/write registers are not affected by Software Reset.
2. Force each clock domain to remain in reset for 64 local clock domain cycles and then begin operation.

NOTE: Software Reset will not reset the analog parts of the Clocks or ADC.

4.3 Analog Front End

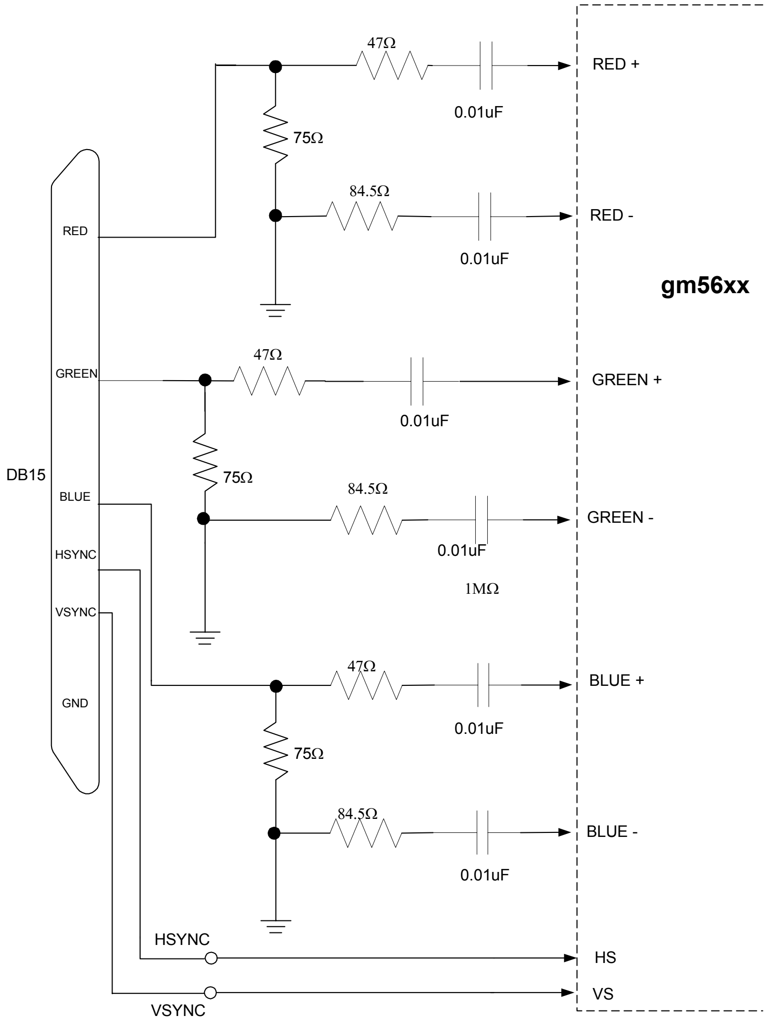
4.3.1 ADC Pin Connection

The analog RGB signals are connected to the device as described below:

Table 12: Pin Connection for RGB Input with HSYNC/VSYNC

Pin Name	ADC Signal Name
Red+	Red
Red-	Terminate as illustrated in the figure below.
Green+	Green
Green-	Terminate as illustrated in the figure below.
Blue+	Blue
Blue-	Terminate as illustrated in the figure below.
HSYNC	Horizontal Sync. Terminate as illustrated in the figure below.
VSYNC	Vertical Sync. Terminate as with HSYNC illustrated in the figure below.

Figure 16: Example ADC Signal Terminations



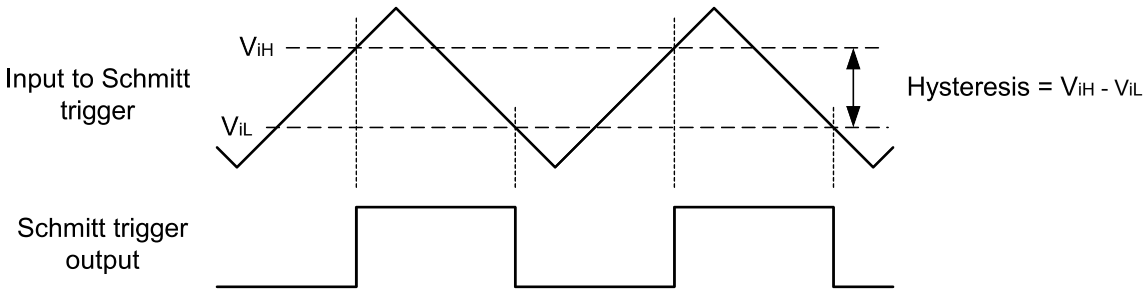
The device does not contain a dedicated SOG input for the sync extraction purpose when the incoming signal format is Sync-On-Green. Instead, the sync extraction block monitors the GREEN channel and performs the required operation.

Note that it is important to follow the recommended layout guidelines for graphics signal interfacing from compatible sources (see the system layout guidelines).

4.3.2 Schmitt Trigger

Integrated Schmitt triggers are used for Horizontal and Vertical Sync inputs. This eliminates the need to use external Schmitt components on the system design. Typical behavior of an integrated Schmitt circuit is shown in the following figure. The integrated Schmitt circuit has 2 sets of threshold voltages for ViH and ViL, which together allows four different hysteresis levels. The Schmitt threshold levels of integrated circuits are in compliance with standard CMOS and TTL input signals. A programmable option is provided in the software for the selection of Schmitt levels.

Figure 17: Schmitt Circuit Timing Diagram



4.3.3 DC Restoration

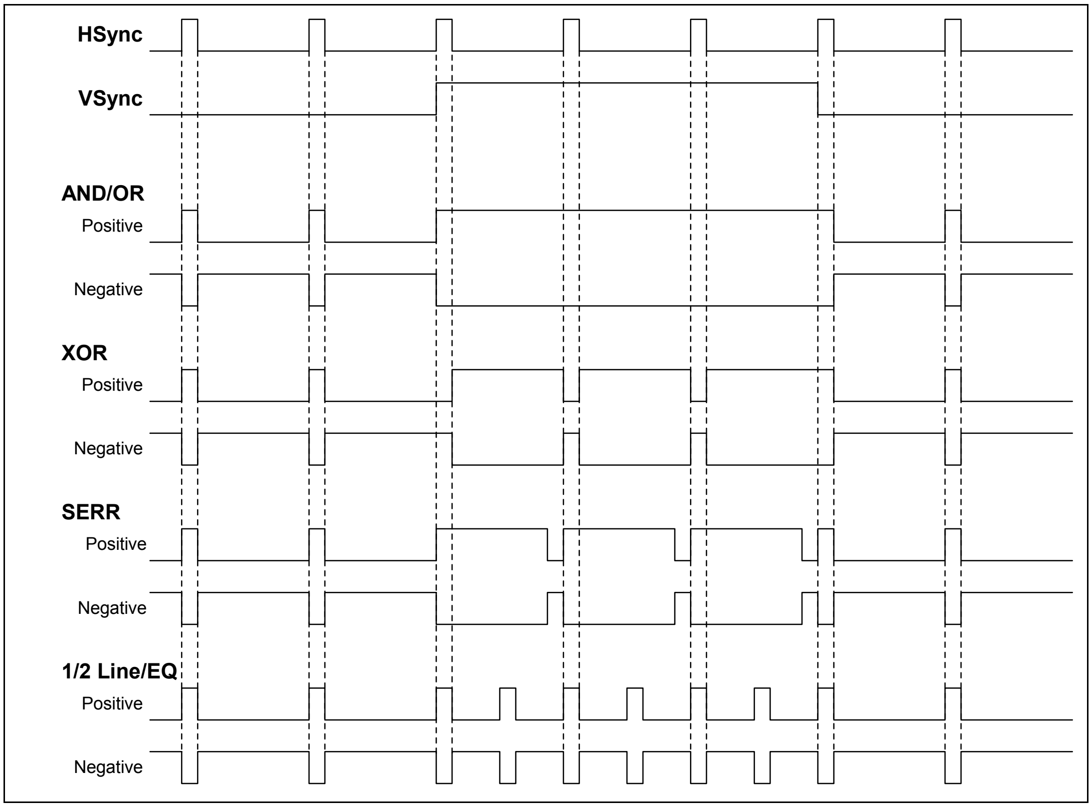
The various analog inputs generated from different graphics sources may have DC offsets. It is necessary to remove the DC offsets by AC coupling these signals through capacitive filters, as recommended in the earlier diagram. Analog Front End provides a means to remove DC offsets so that the full dynamic range of the ADC can be used. Typically, this is achieved by clamping the input signal during the horizontal front porch region. Full control over any such clamping pulse is provided so that the position and size can be controlled via programmable registers.

4.3.4 Sync Extraction

The composite sync pattern may be input on either the HSync input pin or be embedded into GREEN channel. An internal sync stripper is responsible for extracting composite sync signals or SOG signals. Input measurement circuitry is used to determine the polarity and whether the sync signals are separate Hsync / VSync, composite sync or sync on GREEN.

gm56xx devices have the capability to support the following types of SOG and CSYNC inputs.

Figure 18: Composite Sync Support



4.3.5 ADC Characteristics

Table 13: ADC Characteristics

	MIN	TYP	MAX	NOTE
Track & Hold Amp Bandwidth			290 MHz	Guaranteed by design. Note that the Track & Hold Amp Bandwidth is programmable. 290 MHz is the maximum setting.
Full Scale Adjust Range at RGB Inputs	0.55 V		0.90 V	
Full Scale Adjust Sensitivity		+/- 1 LSB		Measured at ADC Output. Independent of full scale RGB input.
Zero Scale Adjust Sensitivity		+/- 1 LSB		Measured at ADC Output.
Sampling Frequency (Fs)	10 MHz		162.5 MHz	
Differential Non-Linearity (DNL)		+/-0.5 LSB	+/-0.9 LSB	Fs = 135 MHz
No Missing Codes				Guaranteed by test.
Integral Non-Linearity (INL)		+/- 1.5 LSB		Fs =135 MHz
Channel to Channel Matching		+/- 0.5 LSB		

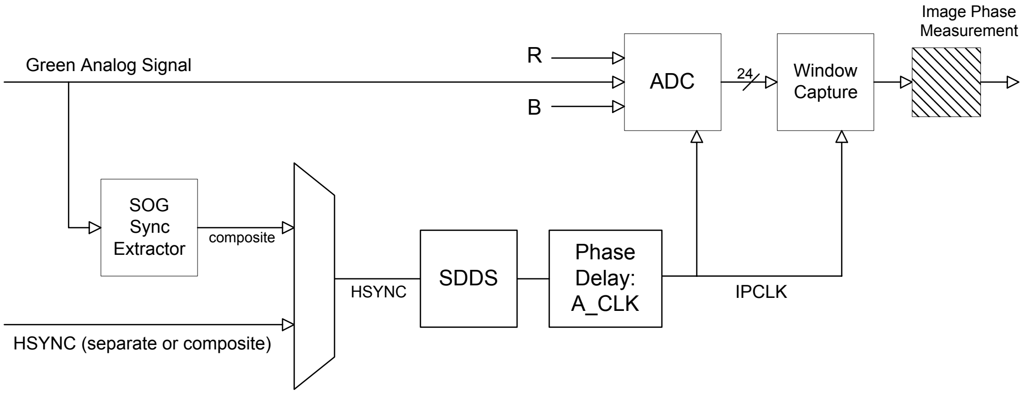
Input formats with resolutions or refresh rates higher than that supported by the LCD panel are displayed as recovery modes only. This is called RealRecovery™. For example, it may be necessary to shrink the image. This may introduce image artifacts. However, the image is clear enough to allow the user to change the display properties.

4.3.6 Clock Recovery Circuit

The SDDS (Source Direct Digital Synthesis) clock recovery circuit generates the clock used to sample analog RGB data (IP_CLK or source clock). SDDS is also used for capturing video (up to 150MHz closed loop for HD, 160MHz openloop for SD). This circuit is locked to the HSYNC of the incoming video signal.

Patented digital clock synthesis technology makes the clock circuits resistant to temperature/voltage drift. Using DDS (Direct Digital Synthesis) technology, the clock recovery circuit can generate any IP_CLK clock frequency within the range of 10MHz to 165MHz.

Figure 19: Clock Recovery



4.3.7 Sampling Phase Adjustment

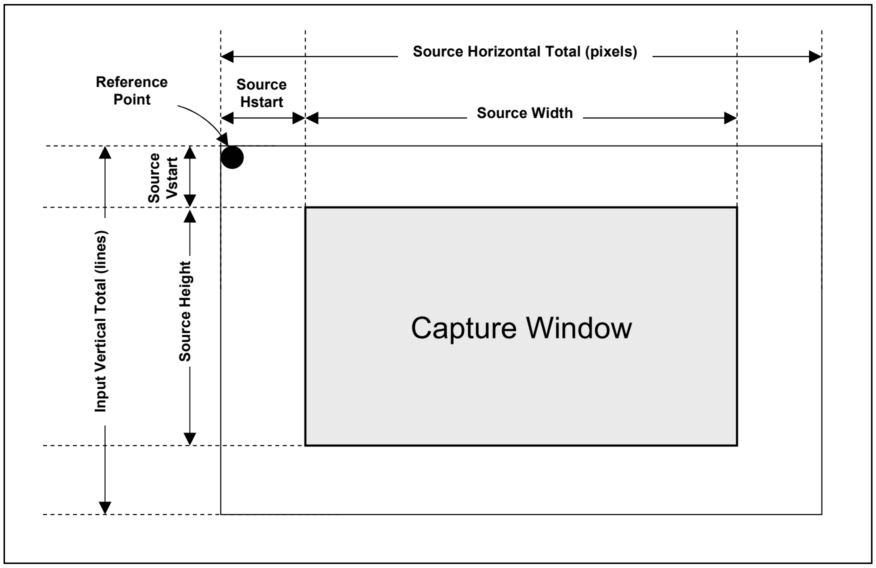
The programmable ADC sampling phase is adjusted by delaying the SDDS clock with respect to the HSYNC input. The accuracy of the sampling phase is checked and the result is read from a register. This feature enables accurate auto-adjustment of the ADC sampling phase.

4.3.8 ADC Capture Window

The capture window is defined by IP_CLKs (equivalent to a pixel count) in the horizontal direction, and defined by lines in the vertical direction. All parameters beginning with “Source” are programmed registers values.

NOTE: The Input Vertical Total is determined solely by the input and is not a programmable parameter.

Figure 20: ADC Capture Window



The Reference Point in the ADC Capture Window figure marks the leading edge of the first internal HSYNC following the leading edge of an internal VSYNC. Both the internal HSYNC and the internal VSYNC are derived from external HSYNC and VSYNC inputs.

Horizontal parameters are defined in terms of single pixel increments relative to the internal horizontal sync. Vertical parameters are defined in terms of single line increments relative to the internal vertical sync.

ADC interlaced inputs may be programmed to automatically determine the field type (even or odd) from the VSYNC/HSYNC relative timing. For more information, see the Input Format Measurement section.

4.3.9 Instant Auto

Instant Auto (patent-pending) is a new auto image adjustment technology from Genesis Microchip. It automatically configures frequency and phase based on the features of the incoming video signal.

Instant Auto advantages:

- Performs auto adjustments faster and more accurately than current conventional methods.
- Performs auto adjustments on full width and partial width images.
- Performs auto adjustments on DOS screens and moving images, such as screen savers and motion pictures.

For further information, refer to the *Instant Auto Application Brief* (C5621-APB-01).

4.4 Ultra-Reliable Digital Visual Interface Receiver (DVI Rx)

The Ultra-Reliable DVI™ receiver block is compliant with DVI 1.0 single link specifications. Digital Visual Interface (DVI) is a standard. This block supports an input clock frequency ranging from 20 MHz to 165 MHz.

4.4.1 DVI Receiver Characteristics

It is very important to follow the recommended layout guidelines for these signals.

Table 14: DVI Receiver Characteristics

	MIN	TYP	MAX	NOTE
DC Characteristics				
Differential Input Voltage	150mV		1200mV	
Input Common Mode Voltage	AVDD –300m V		AVDD -37mV	
Behavior when Transmitter Disable	AVDD -10mV		AVDD +10mV	
AC Characteristics				
Input clock frequency	20 MHz		165 MHz	
Input differential sensitivity (Peak-to-peak)	150mV			
Max differential input (peak-to-peak)			1560 mV	
Allowable Intra-Pair skew at Receiver			250 ps	Input clock = 160 MHz
Allowable Inter-Pair skew at Receiver			4.0 ns	

Through register programming, the receiver unit may be placed in one of three states:

- **Active:** The receiver block is fully on and running.
- **Standby:** RC (clock) channel and the data channel carrying syncs remain active. Data and other control signals are not decoded.
- **Off:** The receiver block is powered down.

4.4.2 High-Bandwidth Digital Content Protection (HDCP)

NOTE: This section applies to the HDCP enabled version of the chip only. HDCP is disabled in the non-HDCP enabled version.

The HDCP system allows authentication of a video receiver by a video transmitter, decryption of transmitter-encoded video data by the receiver, and periodic renewability of authentication during transmission. The circuitry is implemented to allow full support of the HDCP 1.0 protocol for DVI inputs.

For enhanced security, Genesis provides a means of storing and accessing the secret key given to individual monitor units in an encrypted format.

Further details of the protocol and theory of the system can be found in the High-bandwidth Digital Content Protection System specification (see www.digital-cp.com).

4.5 Input Capture

The Input Capture block is responsible for extracting valid data from the input data stream and creating the synchronization signals required by the data pipeline. This block also provides stable timing when no stable input timing exists.

The selected input data stream is cropped using a programmable input capture window. Only data within the programmable window is allowed through the data pipeline for subsequent processing. Data that lies outside of the window is ignored.

4.5.1 Source Standalone Mode

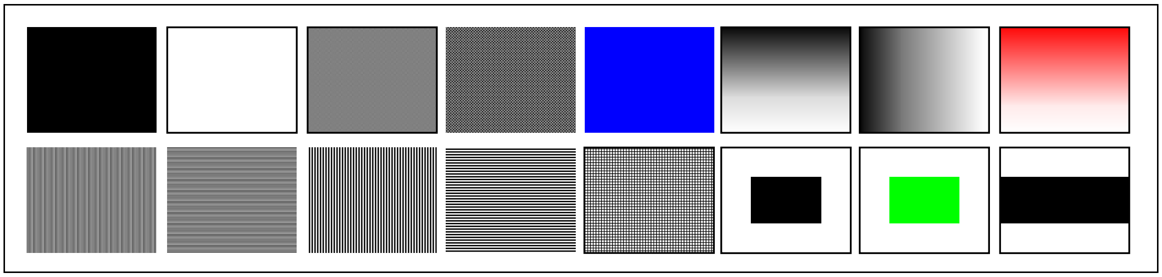
In Source Standalone Mode the Input Capture block produces all input timing. This allows OSD and test patterns to be displayed even when there is no stable input timing present.

Source Standalone Mode can be entered either automatically when input timing goes unstable beyond programmable thresholds or forced by programming a register bit. In this mode, unless a test pattern is being displayed, the active data specified by the Input Capture Window is forced to a programmable color.

4.6 Test Pattern Generator (TPG)

Once programmed, the integrated test pattern generator can replace a video source (e.g. a PC) during factory calibration and test. This simplifies the test procedure and eliminates the possibility of image noise being injected into the system from the source. Foreground and background colors are programmable, and the OSD controller can be used to produce other patterns.

Figure 21: Built-in Test Pattern Examples



4.7 Input Format Measurement

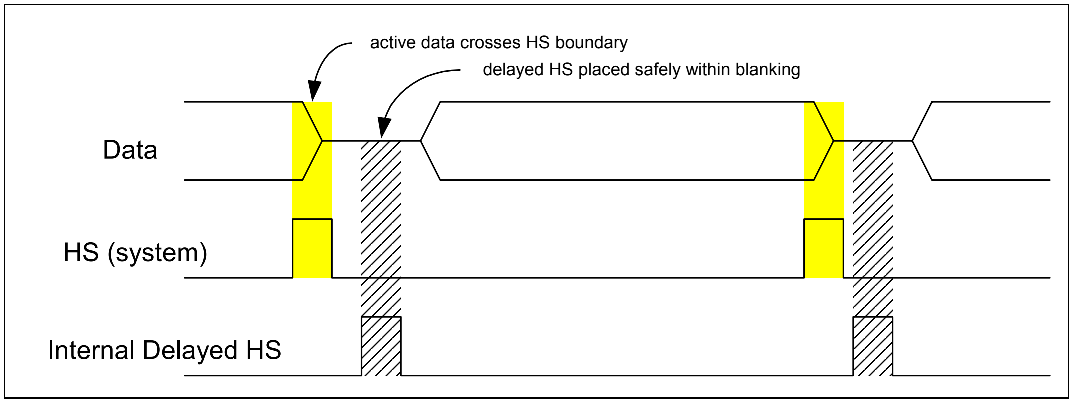
The Input Format Measurement block (IFM) provides the capability of measuring the horizontal and vertical timing parameters of the input video source. Horizontal measurements are measured in terms of the selected IFM_CLK (either TCLK or RCLK/4), while vertical measurements are measured in terms of HSYNC pulses. This information is used to determine the video format and to detect a change in the input format. It is also capable of detecting the field type of interlaced formats.

The IFM features a programmable reset, separate from the regular soft reset. This reset disables the IFM, reducing power consumption. The IFM is capable of operating during power down mode.

HSYNC / VSYNC Delay

The active input region captured is specified with respect to internal HSYNC and VSYNC. By default, internal syncs are equivalent to the HSYNC and VSYNC at the input pins and thus force the captured region to be bounded by external HSYNC and VSYNC timing. However, an internal HSYNC and VSYNC delay feature removes this limitation. The HSYNC and VSYNC delay is used for image positioning of ADC input data. HSYNC is delayed by a programmed number of selected input clocks.

Figure 22: Active Data Crosses HSYNC Boundary


active data crosses HS boundary
delayed HS placed safely within blanking
Data
HS (system)
Internal Delayed HS

Horizontal and Vertical Measurement

The IFM is able to measure the horizontal period and active high pulse width of the HSYNC signal, in terms of the selected clock period (either TCLK or RCLK/4.). Horizontal measurements are performed on only a single line per frame (or field). The line used is programmable. It is able to measure the vertical period and VSYNC pulse width in terms of rising edges of HSYNC. Once enabled, measurement begins on the rising VSYNC and is completed on the following rising VSYNC. Measurements are made on every field / frame until disabled.

Format Change Detection

The IFM is able to detect changes in the input format relative to the last measurement and then alert both the system and the on-chip microcontroller. The microcontroller sets a measurement difference threshold separately for horizontal and vertical timing. If the current field / frame timing is different from the previously captured measurement by an amount exceeding this threshold, a status bit is set. An interrupt can also be programmed to occur.

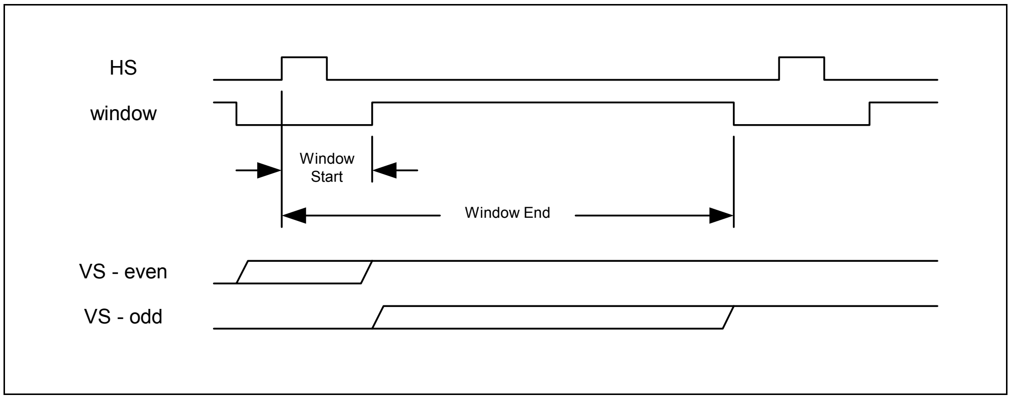
IFM Watchdog

The watchdog monitors input VSYNC and HSYNC. When any HSYNC period exceeds the programmed timing threshold (in terms of the selected IFM_CLK), the counter times out indicating loss of sync. When any VSYNC period exceeds the programmed timing threshold (in terms of HSYNC pulses), the VSYNC watchdog counter times out indicating loss of sync. Both of these events set individual register bits. The time-out status can be read by the OCM, or an interrupt can also be programmed to occur under this condition.

Internal Odd/Even Field Detection (For Interlaced Inputs to ADC Only)

The IFM has the ability to perform field decoding of interlaced inputs to the ADC. The user specifies start and end values to outline a "window" relative to HSYNC. If the VSYNC leading edge occurs within this window, the IFM signals the start of an ODD field. If the VSYNC leading edge occurs outside this window, an EVEN field is indicated (the interpretation of odd and even can be reversed). The window start and end points are selected from a predefined set of values.

Figure 23: ODD/EVEN Field Detection



Input Pixel Measurement

Pixel measurement functions are provided to assist in configuring system parameters such as pixel clock, SDDS sample clocks per line and phase setting, centering the image, or adjusting the contrast and brightness.

Image Phase Measurement

This function measures the sampling phase quality over a selected active window region. This feature may be used when programming the source DDS to select the proper phase setting.

Image Boundary Detection

Image boundary detection is used when programming the Active Window and centering the image. Functions perform measurements to determine the image boundary.

Image Auto Balance

Image auto balance functions perform MIN and MAX pixel value measurements on the input data that is used to adjust brightness and contrast.

4.8 Intelligent Image Processing™ Zoom/Shrink/Sharpening Filter

4.8.1 Variable Zoom Scaling

The scaling engine uses an advanced third generation multi-tap, non-linear scaling engine, which uses FIR filter technique and can accept nearly any input resolution and can scale it to any output resolution, in a range from one-half reduction to a 256-fold expansion. Scaling is highly configurable, with options to scale in both horizontal and vertical directions with different methods. The scalar must scale nearly any signal input to accommodate nearly any panel input. Moreover, it provides high quality scaling of real time video and graphics images. An input field/frame is scalable in both the vertical and horizontal dimensions.

Interlaced fields may be spatially de-interlaced by vertically scaling and repositioning the input fields to align with the output display's pixel map.

4.8.2 Horizontal and Vertical Shrink

A shrink function may be performed on the input data. This is an arbitrary horizontal/vertical reduction to between (50% + 1 pixel/line) to 100% of the input. For example, this allows UXGA 1600x1200 pixels to be displayed as SXGA 1280x1024. For example, this is useful to allow the user to use Windows Display Properties to reduce the screen resolution if it is higher than that of the display.

4.8.3 Programmable Sharpening Filter

The coefficients used in the scaling engine are programmable and can be used to perform sharpening. For example, font edges can be enhanced in text or spreadsheet applications, or motion video images can be sharpened. This is available at any scale factor, or when scaling is not required (i.e. 1:1 mode).

4.8.4 Gamma Look-Up-Table (LUT)

An 8 to 10-bit look-up table (LUT) for each input color channel is intended for Gamma correction and to compensate for a non-linear response of the LCD panel. A 10-bit output results in an improved color depth control. The 10-bit output is then dithered down to 8 bits (or 6 bits) per channel at the display. The LUT is user-programmable to provide an arbitrary transfer function. Gamma correction occurs after the zoom / shrink scaling block. If bypassed, the LUT does not require programming.

4.8.5 Color Standardization and sRGB Support

Internet shoppers may be very picky about what color they experience on the display. RealColor™ digital color controls can be used to make the color response of an LCD monitor compliant with standard color definitions, such as sRGB. sRGB is a standard for color exchange proposed by Microsoft and HP (see www.srgb.com). RealColor controls can be used to make LCD monitors sRGB compliant, even if the native response of the LCD panel itself is not. For more information on sRGB compliance using Genesis devices refer to the *sRGB Application Brief* (C5115-APB-02).

4.9 Display Output Interface

The Display Output Port provides data and control signals that permit the connection to a variety of flat panel devices using LVDS interface. The output interface is configurable for single or dual wide LVDS in 18 or 24-bit RGB pixels format. All display data and timing signals are synchronous with the DCLK display clock. The integrated LVDS transmitter is programmable to allow the data and control signals to be mapped into any sequence depending on the specified receiver format. DC balanced operation is supported as described in the Open LDI standard.

4.9.1 Display Synchronization

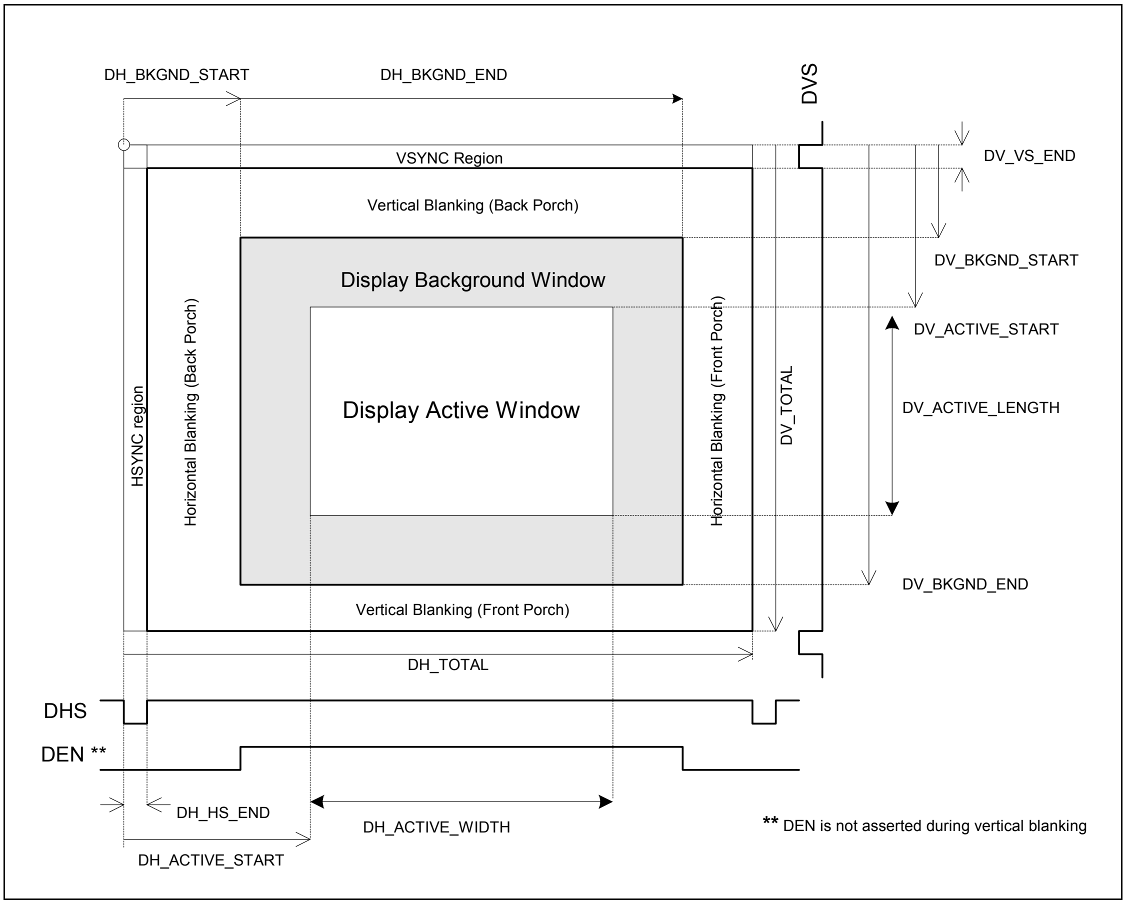
The following display synchronization modes are supported:

- **Frame Sync Mode:** The display frame rate is synchronized to the input frame or field rate. This mode is used for standard operation.
- **Free Run Mode:** No synchronization. This mode is used when there is no valid input timing (i.e. to display OSD messages or a splash screen) or for testing purposes. In free-run mode, the display timing is determined only by the values programmed into the display window and timing registers.

4.9.2 Display Timing Programming

Horizontal values are programmed in single-pixel increments relative to the leading edge of the horizontal sync signal. Vertical values are programmed in line increments relative to the leading edge of the vertical sync signal.

Figure 24: Display Windows and Timing



Display Active Window

Data captured by the Input Capture Window and processed by the various image manipulation blocks is output in the Display Active Window. This window is always in the foreground and lies on top of all other output windows, except OSD overlay windows.

Typically, the Display Active Window is set to the same size as the output of the Scaling Engine. If the Display Active Window is set too small, then the bottom and right hand edges of the image data are cropped. If the Display Active Window is set too large, then the extra space to the left and bottom of the Display Active Window is forced to the Background Window color.

NOTE: A separate register bit is used to control whether the display active window is visible or not.

Display Background Window

The Background Window is a programmable window that specifies the total displayable area on the target flat panel, i.e. region in which data is active. This window is typically programmed to the resolution of the flat panel device. The Display Active Window lies on top of this window, but is cropped by the Background

Window. The Background Window has a programmable color. If the Display Active Window is specified to be smaller than the Background Window, then the programmable color is seen as a background color lying underneath the Display Active Window.

Frame Timing Window

The Frame Timing Window defines the horizontal and vertical totals (i.e. active + blanking) and is typically programmed to the desired panel timing. A register bit is used to define whether output timing is active or not. Disabling output timing completely disables all output timing, i.e. the output data bus and all output timing signals go high impedance.

OSD/Overlay Window

The OSD/Overlay Window can be programmed so that it lies anywhere within the Background Window.

4.9.3 Output Dithering

The Gamma LUT outputs a 10-bit value for each color channel. This value is dithered down to either 8-bits for 24-bit per pixel panels, or 6-bits for 18-bit per pixel panels. In this way it is possible to display 16.7 million colors on a LCD panel with 6-bit column drivers.

The benefit of dithering is that the eye tends to average neighboring pixels and a smooth image free of contours is perceived. Dithering works by spreading the quantization error over neighboring pixels both spatially and temporally. Two dithering algorithms are available: random or ordered dithering. Ordered dithering is recommended when driving a 6-bit panel.

All gray scales are available on the panel output, whether using 8-bit panel (dithering from 10 to 8 bits per pixel) or using 6-bit panel (dithering from 10 down to 6 bits per pixel).

4.9.4 Dual Channel LVDS Transmitter

An integrated LVDS transmitter with programmable input to output configuration is provided to enable drive of all known panels. The LVDS transmitter can support the following:

- Single pixel mode
- 24-bit panel mapping to the LVDS channels
- 18-bit panel mapping to the LVDS channels
- Programmable channel swapping (the clocks are fixed)
- Programmable channel polarity swapping
- Supports up to SXGA 75Hz output

Table 15: Supported LVDS 24-bit Panel Data Mappings

Channel 0	R0, R1, R2, R3, R4, R5, G0
Channel 1	G1, G2, G3, G4, G5, B0, B1
Channel 2	B2, B3, B4, B5, PHS, PVS, PDE
Channel 3	R6, R7, G6, G7, B6, B7, RES

Channel 0	R2, R3, R4, R5, R6, R7, G2
Channel 1	G3, G4, G5, G6, G7, B2, B3
Channel 2	B4, B5, B6, B7, PHS, PVS, PDE
Channel 3	R0, R1, G0, G1, B0, B1, RES

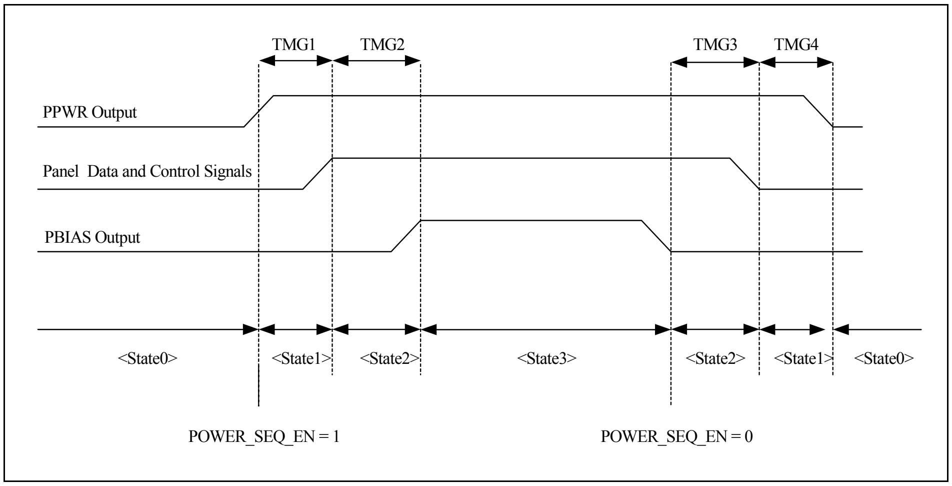
Table 16: Supported LVDS 18-bit Panel Data Mapping

Channel 0	R0, R1, R2, R3, R4, R5, G0
Channel 1	G1, G2, G3, G4, G5, B0, B1
Channel 2	B2, B3, B4, B5, PHS, PVS, PDE
Channel 3	Disabled for this mode

4.9.5 Panel Power Sequencing (PPWR, PBIAS)

Two dedicated outputs (PPWR, PBIAS) control LCD power sequencing once data and control signals are stable. The timing of these signals is fully programmable.

Figure 25: Panel Power Sequencing



4.10 Energy Spectrum Management™ (ESM)

High spikes in the EMI power spectrum may cause LCD monitor products to violate emissions standards. Drive strength control and output clock modulation features have been included to reduce electromagnetic interference (EMI). These features spread EMI energy over a range of frequencies and reduce the concentration of EMI energy.

These features also help to eliminate the costs associated with EMI by reducing components and shielding.

4.11 On-Screen Display (OSD)

An integrated fully programmable, high-quality OSD controller enables the creation and insertion of data that can be used for menus and system information. Graphics used are divided into “cells” of programmable size. The cells are stored in an on-chip static RAM (16K Bytes) and can be stored as 1-bit per pixel data, 2-bit per pixel data or 4-bit per pixel data.

General features of the OSD controller include:

- **Two OSD Rectangles –** The OSD can appear in two separately defined rectangular regions.
- **OSD Position –** The OSD menu can be positioned anywhere on the display region. The reference point is Horizontal and Vertical Display Background Start (DH_BKGND_START and DV_BKGND_START).
- **OSD Stretch –** The OSD image can be stretched horizontally and/or vertically by a factor of two. Pixel and line replication is used to stretch the image.
- **OSD Blending** – Sixteen levels of blending are supported for selected colors in the character-mapped.

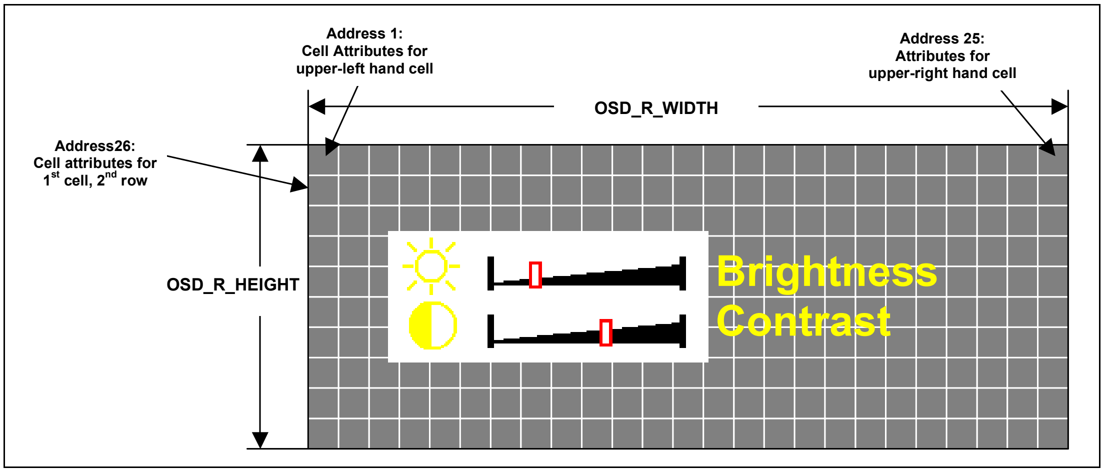
4.11.1 On-Chip OSD SRAM

The on-chip static RAM stores the cell map, cell definitions, and attribute map. The OSD SRAM is shared by the on-chip microcontroller as part of its normal addressable memory space.

In memory, the cell map is organized as an array of words, each defining the attributes of one visible character on the screen starting from upper left of the visible character array. These attributes specify which character to display, whether it is stored as 1, 2 or 4 bits per pixel, the foreground and background colors, blinking, etc.

Registers are used to define the visible area of the OSD image. See the OSD Cell Map figure.

Figure 26: OSD Cell Map



Cell definitions are stored as bit map data. On-chip registers point to the start of 1-bit per pixel definitions, 2-bit per pixel definitions and 4-bit per pixel definitions respectively.

Note that the cell map and the cell definitions share the same on-chip RAM. Thus, the size of the cell map can be traded off against the number of different cell definitions. In particular, the size of the OSD image and the number of cell definitions must fit in RAM.

4.11.2 OSD Color Look-up Table (CLUT)

The Color Look-up Table (CLUT) is stored in an on-chip RAM that is separate from the OSD RAM. Each pixel of a displayed cell is resolved to an 8-bit color code. This selected color code is then transformed to a 24-bit value using a 256x24-bit look up table.

4.12 On-Chip Microcontroller (OCM)

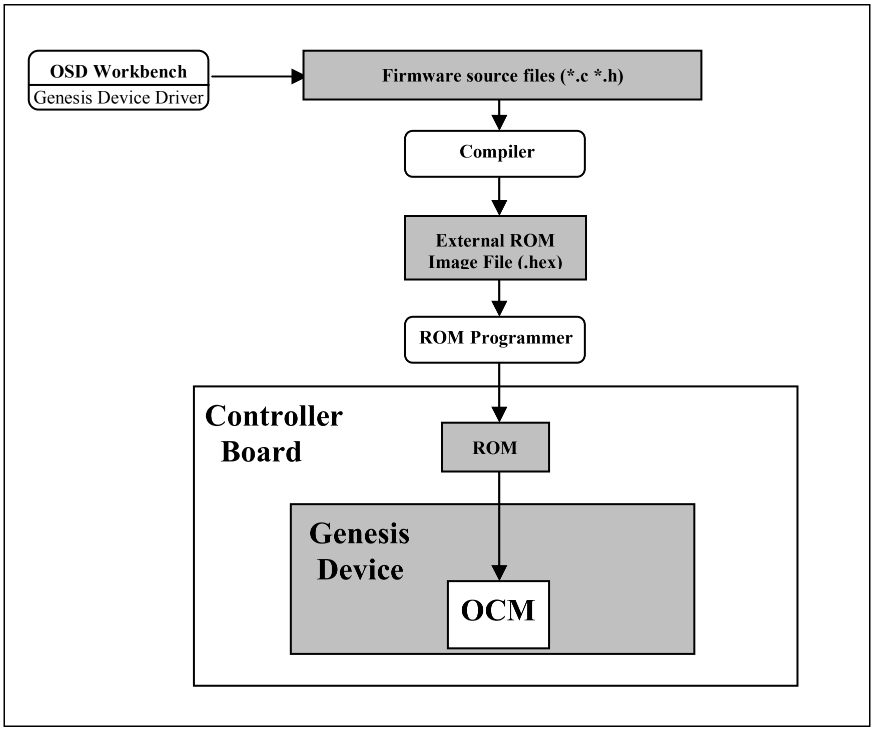
The on-chip microcontroller (OCM) is a 16-bit x86 100MHz processor capable of acting as either the overall system controller or a slave controller, receiving commands from an external controller.

The OCM executes firmware running from external serial ROM, as well as driver-level (or Application Programming Interface – API) functions residing in internal ROM. The serial port connects directly to standard, commercially available SPI ROM or programmable serial FLASH ROM devices from all popular vendors including ATMEL Data FLASH. The cache controller within the device enables the prefetching of data and code from SPI ROM to overcome the bandwidth limitation of low speed

SPI devices. Typical monitor applications need around 64K to 128K Byte serial FLASH devices to store the code and OSD data.

Both firmware and OSD content must be compiled into a HEX file and then loaded onto the external ROM. The OSD content is generated using Genesis Workbench. Genesis Workbench is a GUI-based tool for defining OSD menus, navigation, and functionality.

Figure 27: OCM Programming



Genesis recommends using Paradigm compiler (http://www.devtools.com) to compile the firmware source code into a hex file. This hex file is then downloaded into the external ROM using In-System-Programming (Genesis debug software G-Probe communicates with the OCM, which in turn programs a FLASH ROM in the system using the ROM_WEn signal) or using commercially available ROM programmers.

OCM Watchdog

A hardware watchdog is used to ensure the OCM resets after a programmable delay if the watchdog is not reset. This feature helps to ensure that the OCM does not hang indefinitely.

4.12.1 Embedded Bootstrap Function

An embedded ROM bootstrap function is provided from which to boot when external ROM is not present or does not contain data. It is always recommended to boot from embedded ROM. The OCM_ROM bootstrap selects the initial state of the internal OCM ROM.

The embedded ROM firmware first looks for a 'signature' in external ROM. The 'signature' is the ASCII values for the character string "xROM" starting address. If this signature is found, it performs a CRC check. If CRC is valid, it jumps to the appropriate external ROM address.

If the signature is not present, the embedded firmware does not jump to external ROM. In this case, it runs in its own loop that supports debugging commands (using G-Probe debugging software available from Genesis) over either the UART port or DDC2Bi port.

4.12.2 In-System Programming (ISP) of External FLASH ROM

Hardware support is provided for in-system programming of external FLASH ROM devices. The ROM_WEn pin can be connected to the write enable of the FLASH ROM. The embedded boot firmware performs the writes.

4.12.3 UART Interface

The OCM has an integrated Universal Asynchronous Remote Terminal (UART) port that can be used as a factory debug port. The UART can be used to 1) read / write chip registers, 2) read / write to NVRAM, and 3) read / write to FLASH ROM (In-System Programming).

4.12.4 DDC2Bi Interface

Hardware support is provided for DDC2Bi communication over the DDC channel of the analog input port. The specification for the DDC2Bi standard can be obtained from VESA (www.vesa.org). The DDC2Bi port can be used as a factory debug port or for field programming. In particular, the DDC2Bi port can be used to 1) read / write chip registers, 2) read / write to NVRAM, and 3) read / write to FLASH ROM (In-System-Programming).

4.12.5 JTAG Interface

A JTAG interface is provided to allow in-circuit debugging of the internal OCM. The JTAG interface can operate in 2-wire serial interface mode. A 2-wire to JTAG bridge circuit is provided to allow JTAG commands to be issued using only two pins HOST_SCL and HOST_SDA.

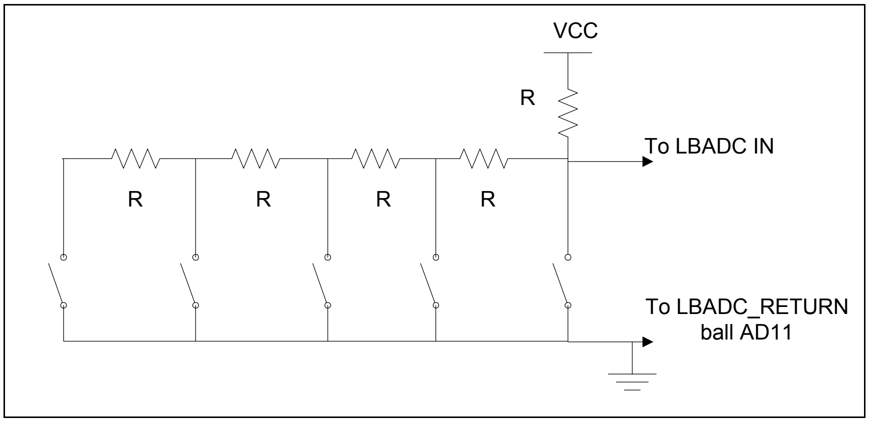
4.12.6 General Purpose Inputs and Outputs (GPIO)

There are seven general-purpose input/output (GPIO) pins available in gm5621 (only available in LVDS versions) for interfacing peripheral devices. In addition, there are seven GPO (output only) pins, two of which are shared with PWM functionality. The general purpose output pins can be configured either as CMOS or open drain type using the control registers. The general purpose signals are used by the OCM to communicate with other devices in the system, such as keypad buttons, NVRAM, LEDs, audio DAC, etc. Each GPIO has independent direction control and open drain enable for reading and writing.

4.12.7 Low-Bandwidth ADC (LBADC)

A general-purpose ADC is integrated to allow for functions such as keypad scanning or for monitoring system temperature or voltage sensors. The ADC has 8 bits of resolution, and can perform a conversion in 13 LBADC clock periods. The LBADC sampling clock can either be TCLK, TCLK/2 or TCLK/4. The maximum sampling clock frequency for 8-bit resolution is 14MHz. An analog multiplexer selects one of three analog input pins as the input to the ADC.

Figure 28: Typical Keypad Function



4.12.8 Low Power State

A low power state provides the ability to disable clocks to selected parts of the chip. The OCM_CLK can also be reduced so that the OCM itself consumes less power for TV standby mode. In this mode, only IR and LB-ADC (keypad) functionality is available to wake up the system.

4.12.9 Pulse Width Modulation (PWM)

Many of today's LCD back light inverters require both a PWM input and variable DC voltage to minimize flickering due to the interference between panel timing and the inverter's AC timing, and adjust brightness. There are two pins available for PWM outputs: PWM0 (GPO4) and PWM1 (GPO5). The duty cycle of these signals is programmable. They may be connected to an external RC integrator to generate a variable DC voltage for a LCD back light inverter. Panel HSYNC is used as the clock for a counter generating this output signal.

4.13 Bootstrap Configuration Pins

During hardware reset, GPO and SPI CSn pins with bootstrap signals are configured as inputs. On the negating edge of RESETn, the value on these pins is latched and stored. This value is readable by the on-chip microcontroller (or external microcontroller via the host interface). Install a 4.7K pull-up or pull-down resistor to indicate logic '1', or '0' status on the bootstrap pins. By default, the bootstrap pins are provided with internal 60KΩ pull-down resistors.

Table 17: Bootstrap Signals

Bootstrap	Pin Name	No	Description
ATMEL_EN	PWM0	50	Configure SPI protocol: 0 = Standard SPI ROM used 1 = ATMEL SPI ROM with proprietary read mode
UART_PIN_SEL	PWM1	119	UART pin mapping select. This determines the initial pin map for the UART at Power-on. UART is enabled. 0 = UART_DI is DDC_SCL_VGA, UART_DO is DDC_SDA_VGA 1 = UART_DI is GPO_2, UART_DO is GPO_3 (Recommended)
INTERFACE_SEL	GPO_0 GPO_3	51 58	Interface Select. Determines the interface to control this device and configures JTAG access [GPO_3, GPO_0] 00 = Internal Micro, SPI as ROM. JTAG enabled on DDC_SDA_DVI and DDC_SCL_DVI only 01 = Internal Micro, SPI as ROM, JTAG disabled 10 = Reserved 11 = Reserved Note: DDC2Bi (DVI or VGA) is available for all settings.
OSC_SEL	GPO_1	56	Selection of TCLK source 0 = Xtal and internal oscillator (Recommended) 1 = TTL oscillator (input on TCLK pin)
OCM_ROM	GPIO_2	57	Selects the initial state of internal OCM ROM 0 = Internal ROM on, and mapped to top 32K of OCM address range. OCM will boot from internal ROM. (Recommended) 1 = Internal ROM off. This is debug mode with the external ROM mapped to the entire upper 512K of the OCM address range. OCM will boot from external ROM.
V_EDID_ATMEL	SPI_CSn	59	Configure Virtual EDID logic for standard or ATMEL type reads when the monitor is powered off. This bootstrap is latched at the application of power to pin DDC_33. 0 = Standard SPI ROM 1 = ATMEL ROM with proprietary read mode

Note: These signals have a 60K ohm on-chip pulldown resistor. Therefore, the bootstrap is 0 by default. A 4.7K ohm pullup is required onboard to set the bootstrap to 1. It is recommended to provide an external pull-down resistor (4.7K) over and above the on-chip pull-down for guaranteed operations over wider temperature range.

5 Electrical Specification

The following targeted specifications have been derived by simulation.

Preliminary DC Characteristics

Table 18: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages (1,2)	$V_{VDD\_3.3}$	-0.3		3.6	V
1.8V Supply Voltages (1.2)	$V_{VDD\_1.8}$	-0.3		1.98	V
Input Voltage (5V tolerant inputs) (1,2)	$V_{IN5Vtol}$	-0.3		5.5	V
Input Voltage (non 5V tolerant inputs) (1,2)	V_{IN}	-0.3		3.6	V
Electrostatic Discharge(4)	V_{ESD}			±2.0	kV
Latch-up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		150	°C
Operating Junction Temperature	T_J	0		125	°C
Thermal Resistance (Junction to Air) Natural Convection (3)	θ_{JA_2L}			44.5	°C/W
Thermal Resistance (Junction to Case) Convection (3)	θ_{JC}			21.1	°C/W
Soldering Temperature (<10 sec.)	T_{SOL}			220	°C
Vapor Phase Soldering (<10 sec.)	T_{VAP}			220	°C
Soldering Temperature (<10 sec.) – Lead-Free	T_{SOL}			250	°C
Vapor Phase Soldering (<10 sec.) – Lead-Free	T_{VAP}			250	°C

NOTE (1): All voltages are measured with respect to GND.

NOTE (2): Absolute maximum voltage ranges are for transient voltage excursions.

NOTE (3): These are simulated results under following conditions - Two layer PCB, No heat spread, Air flow = 0 m/s.

NOTE (4): Electrostatic Discharge (ESD): Integrated ESD diodes are provided to protect the device during handling. External on-board ESD diodes are required on the analog RGB inputs, and DDC inputs for protection against electrical overstress (EOS). The ESD result shown is not applicable for reserved pins.

Table 19: DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Power					
Power Consumption @ 135 MHz	P_{SXGA}		1.0	1.1	W
Power Consumption @ Low Power Mode (1)	P_{LP}		95		mW
3.3V Supply Voltages (AVDD and RVDD)	$V_{VDD\_3.3}$	3.15	3.3	3.45	V
1.8V Supply Voltages (VDD and CVDD)	$V_{VDD\_1.8}$		1.8		V
Supply Current @ CLK =135MHz (gm56xx) • 1.8V digital supply (2) • 1.8V analog supply (3) • 3.3V digital supply (4) • 3.3V analog supply (5)	I $I_{VDD\_1.8}$ $I_{AVDD\_1.8}$ $I_{VDD\_3.3}$ $I_{AVDD\_3.3}$		440	 243 21 82 110	mA
Supply Current @ Low Power Mode*	I_{LP}		40		mA

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
High Voltage	V_{IH}	2.0		V_{DD}	V
Low Voltage	V_{IL}	GND		0.8	V
Clock High Voltage	V_{IHC}	2.4		V_{DD}	V
Clock Low Voltage	V_{ILC}	GND		0.4	V
High Current (V_{IN} = 5.0 V)	I_{IH}	-25		25	μA
Low Current (V_{IN} = 0.8 V)	I_{IL}	-25		25	μA
Capacitance (V_{IN} = 2.4 V)	C_{IN}			8	pF
Outputs					
High Voltage (I_{OH} = 7 mA)	V_{OH}	2.4		V_{DD}	V
Low Voltage (I_{OL} = -7 mA)	V_{OL}	GND		0.4	V
Tri-State Leakage Current	I_{OZ}	-25		25	μA

NOTE (1): Low power figures indicates that system is in sleep (low power mode) where MCU is On and checking for the input signal activity.
NOTE (2): Includes all CVDD_18 pins.
NOTE (3): Includes VDD_ADC_18, VDD_DVI_18 and VDD_RPLL_18 pins.
NOTE (4): Includes all RVDD_33 and AVDD _OUT_33 pins.
NOTE (5): Includes pins VDDA_ADC_33, VDDA_DVI_33 and AVDD_RPLL_33 pins.

NOTE (6): Maximum current figures are provided for the purposes of selecting a power supply circuit.

Preliminary AC Characteristics

All timing is measured to a 1.5V logic-switching threshold. The minimum and maximum operating conditions used were: TDIE = 0 to 125° C, Vdd = 2.35 to 2.65V, Process = best to worst, CL = 16pF for all outputs.

Table 20: Max Speed of Operation

Clock Domain	Max Speed of Operation
Main Input Clock (T_CLK)	24 MHz (14.3MHz recommended)
ADC Clock (S_CLK)	165 MHz
Input Clock (IP_CLK)	165 MHz
Reference Clock (R_CLK)	220MHz (200MHz recommended)
On-Chip Microcontroller Clock (OCM_CLK)	100 MHz
Display Clock (D_CLK)	135 MHz

Table 21: SPI Interface Timing, VDD = 2.7~3.6V

Symbol	Parameter	Min	Max	Units
F_{CLK}	Serial Clock frequency		50	MHZ
T_{SCKH}	Serial Clock High Time	5		ns
T_{SCKL}	Serial Clock Low Time	5		ns
T_{SCKR}	Serial Clock Rise Time		5	ns
T_{SCKF}	Serial Clock Fall Time		5	ns
T_{CES}	CE# active Setup time	10		ns
T_{CEH}	CE# active Hold time	10		ns
T_{CHS}	CE# Not active Setup time	10		ns
T_{CHH}	CE# Not active Hold time	10		ns
T_{CPH}	CE# High time	100		ns
T_{CHZ}	CE# High to High-Z output		20	ns
T_{CLZ}	SCK Low to Low-Z Output	0		ns
T_{DS}	Data In Setup Time	5		ns
T_{DH}	Data In Hold Time	5		ns
T_{OH}	Output Hold from SCK change	0		ns
T_{V}	Output Valid from SCK		20	ns
T_{SE}	Sector Erase		25	ms
T_{BE}	Block Erase		25	ms
T_{SCE}	Chip Erase		100	ms
T_{BP}	Byte Program		20	µs

Figure 29: gm56xx SPI Output or Serial Interface SPI ROM Input Timing

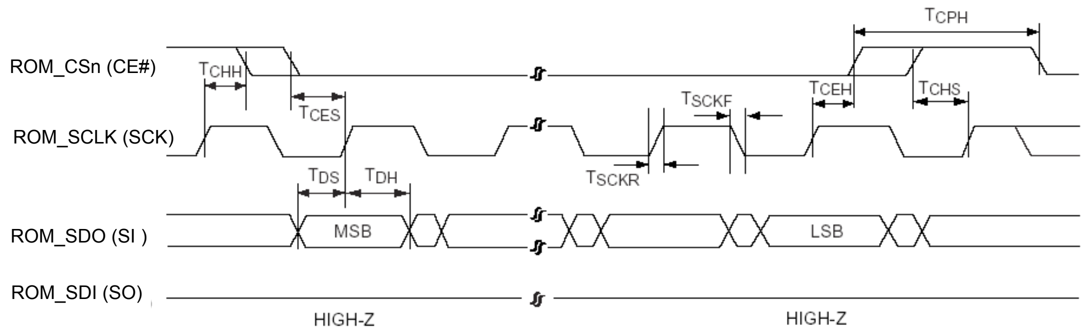


Figure 30: gm56xx Input or Serial Interface SPI ROM Output Timing

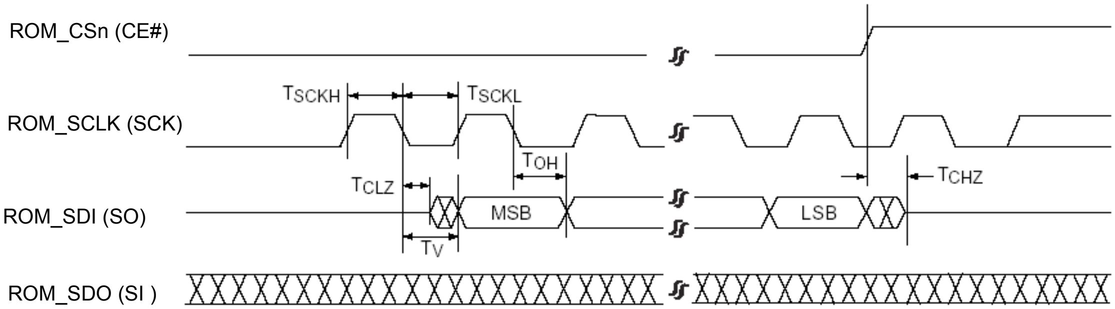


Figure 31: LVDS Transmitter Switching Characteristics

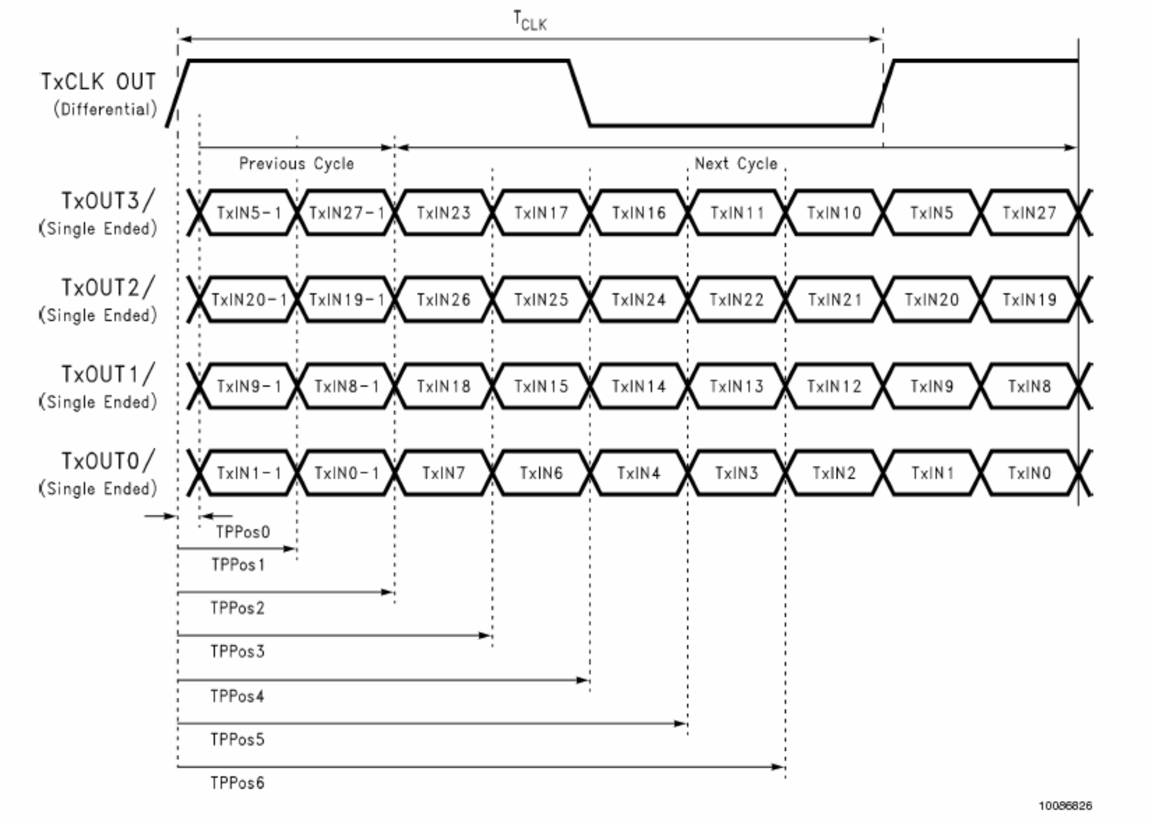


Table 22: LVDS Even Channels 0 to 3(1)

Symbol	Parameters	E_CH0 ~ E_CH3	Typical	Units
TPPos0	T/X output pulse position for bit 0	F= 65 Mhz	-0.1	ns
TPPos1	T/X output pulse position for bit 1		2.1	ns
TPPos2	T/X output pulse position for bit 2		4.3	ns
TPPos3	T/X output pulse position for bit 3		6.5	ns
TPPos4	T/X output pulse position for bit 4		8.7	ns
TPPos5	T/X output pulse position for bit 5		10.9	ns
TPPos6	T/X output pulse position for bit 6		13.1	ns

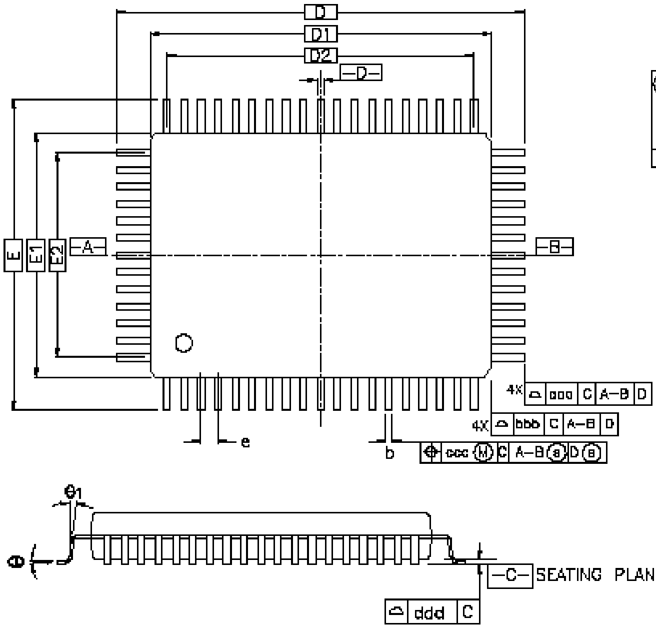
Table 23: LVDS Odd Channels 0 to 3(1)

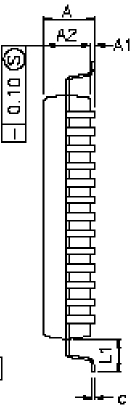
Symbol	Parameters	O_CH0 ~ O_CH3	Typical	Units
TPPos0	T/X output pulse position for bit 0	F= 65 Mhz	-0.3	ns
TPPos1	T/X output pulse position for bit 1		1.9	ns
TPPos2	T/X output pulse position for bit 2		4.1	ns
TPPos3	T/X output pulse position for bit 3		6.3	ns
TPPos4	T/X output pulse position for bit 4		8.5	ns
TPPos5	T/X output pulse position for bit 5		10.7	ns
TPPos6	T/X output pulse position for bit 6		12.9	ns

NOTE: There is +/- 200 ps variation for the measurements for even and odd channels.

6 Package Specification

gm56xx 128 Pin PQFP Package Drawing

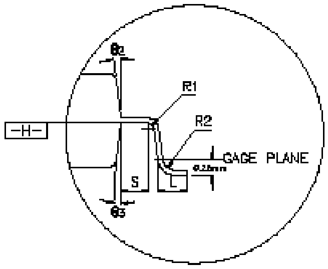




COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A_1	0.25	—	—	0.010	—	—
A_2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D_1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E_1	14.00 BASIC			0.551 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
ALLOY 42 L/F θ_2 , θ_3	7° REF			7° REF		
COPPER L/F θ_2 , θ_3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		



Notes:

1. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H- .

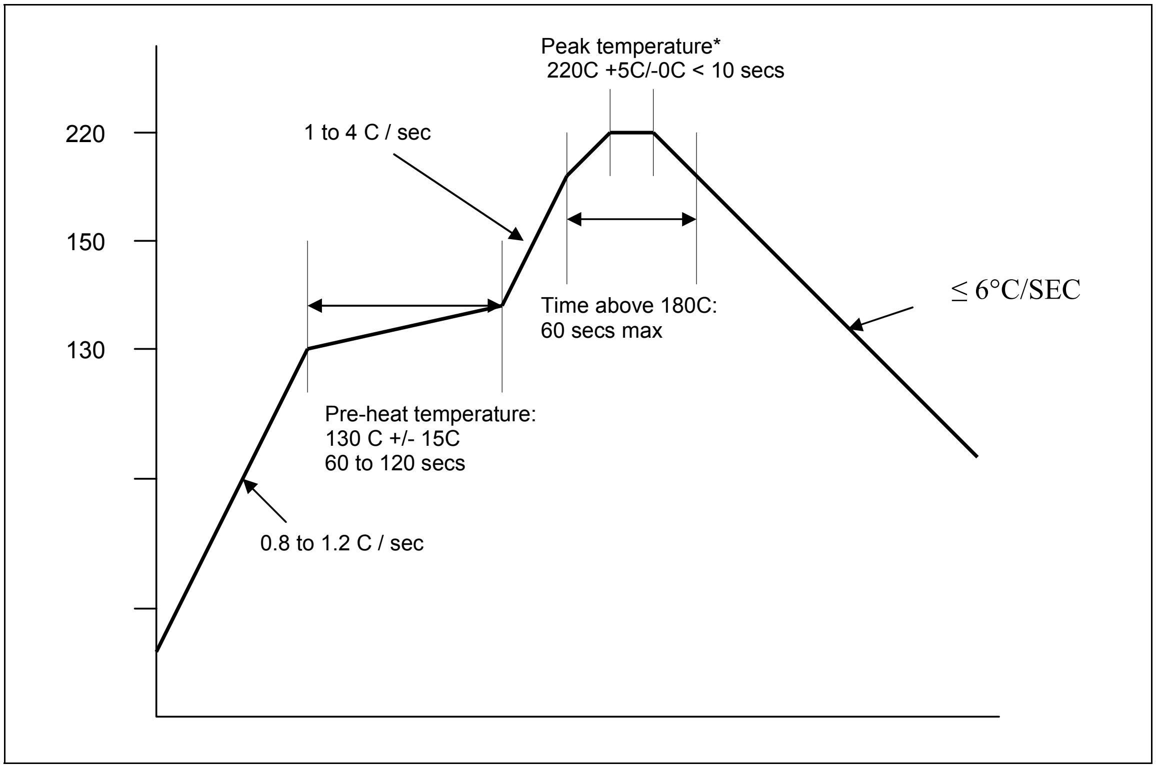
2. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion can be 0.08mm total in excess of dimension b at maximum material condition. Dambar cannot be located on the lower radius or the lead foot

7 Solder Profiles

7.1 Regular QFP Reflow Profile

The following is the recommended solder reflow profile for Genesis Microchip regular QFP devices.

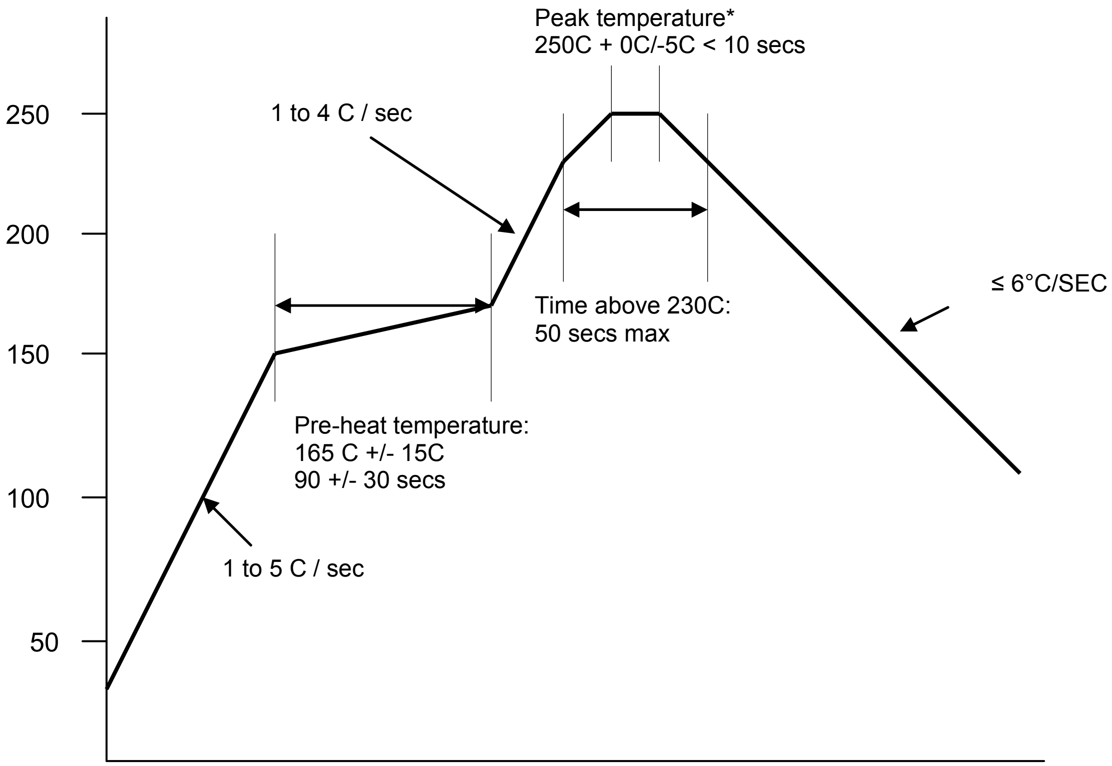
Figure 32: Regular QFP Solder Reflow Profile



7.2 Lead-Free QFP Reflow Profile

The following is the recommended solder reflow profile for Genesis Microchip lead-free QFP devices.

Figure 33: Lead-Free QFP Solder Reflow Profile

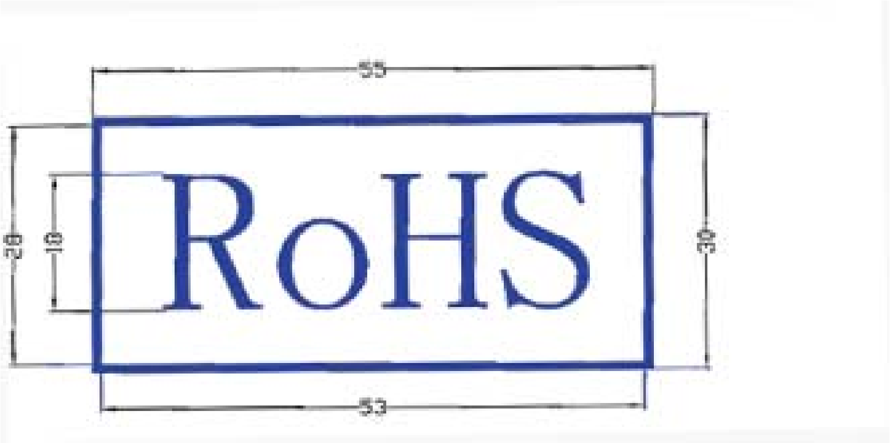


*Peak temperature:

208QFP, 168QFP, 128QFP, 100QFP max temperature = 250C + 0C/-5C

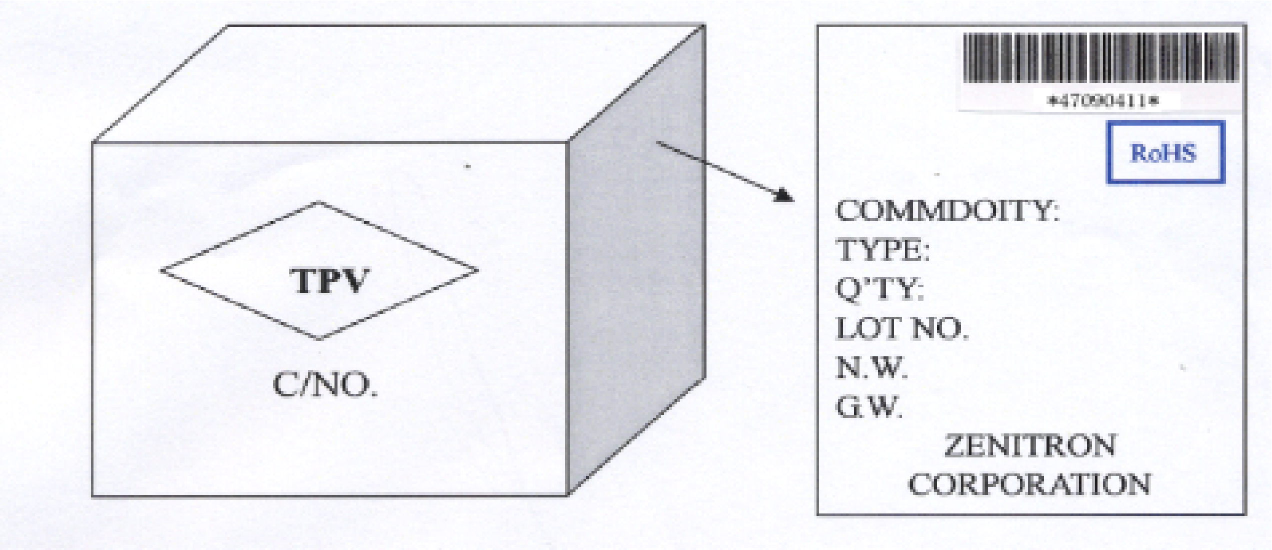
GENESIS

Label Size



字體：藍色宋體”RoHS”需垂直居中，水平居中

#Carton



Carton size:Anomaly

#TPV RoHS product stick RoHS blue word seal on the upper-right corner of the side mark of carton

GENESIS

To: Top Victory Electronics (Fujian) Co.,Ltd

Date: 1/12/05

Company: Genesis Micro Chip
Address: 2150 Gold St, Alviso,
CA, 95002
Product name:

Guarantee of compliance regarding six Hazardous Substances

Top Victory Electronics (Fujian) Co.,Ltd

We (includes our subsidiary, affiliated company) here guarantee that all the components and parts shipped to you (includes directly shipping or via third parties) are in accordance with below limitation.

	Hazardous substance	limitation
1.	Cadmium and cadmium compounds	5ppm
2.	Lead and lead compounds	100ppm (For solder bar:1000ppm)
3.	Mercury and mercury compounds	1000ppm
4.	Hexavalent chromium compounds	1000ppm
5.	Polybrominated biphenyls (PBB)	1000ppm
6.	Polubrominated diphenylethers (PBDE)	1000ppm
7.	$Cd+Pb+Hg+Cr^{+6}$	100ppm (Only for packing material together with TPV production to market.)

Note:

1. Please refer to file named "specification and explanation relating with hazardous substance of TPV.PPT" for exemption items from the requirements of applications of lead, mercury, cadmium and hexavalent chromium.
2. In witness where of the above Guarantee has been duly exercised by the company's fully authorized representative signed below.

Signature:

Name: Masood Kafi

*Need to affix the official seal, afford by the post or fax.

Raw Material and Raw Material Supplier Questionnaire

Product Type:

TPV Part No	Product name	Name of Parts/raw material/subsidiary material	Supplier Name	Address (approximately)	Cd (ppm)	SGS or ITS Test Report No.	Pb (ppm)	SGS or ITS Test Report No.	Cr6+ (ppm)	SGS or ITS Test Report No.	Hg (ppm)	SGS or ITS Test Report No.	PBB/PBDE (ppm)	SGS or ITS Test Report No.
	GMxxxx-LF-xx series		Genesis Micro-chip	2150 Gold St, Alviso, CA 95002	0	KA/2003/50118	0	KA/2003/50118	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	[redacted]

Note:
1. Please fill in this table with detailed information of all components/raw material/
subsidiary material used in above product.
2. Please in detail and correctively fill with relevant supplier name and type name.
3. Please fill in 6 kinds Environment Management Substance content and according to
test report No. of fair and square third party test organization such as SGS or

Signature/Positic , Customer Quality Manager

Company Name: Genesis Micro-Chip

Stamp:

AOC
EYES VALUE
研发处
Top Victory Electronics(Fujian) Co.,Ltd. Shangzheng Yuanhong Road,Fuqing,Fujian, China Tel: (0591)5285555 5285446 Fax: (0591)5285447
冠捷电子(福建)有限公司. 福建省福清市元洪路上郑 E-mail: xiejg@tpv.com.cn web site:http://www.tpv.com.cn

RoHS 零件耐焊接热标准

版本：A 发布时间：May-18-04 编写：May-17-04 核准：May. 17. 04

1．波峰焊接零件

适用范围：所有通过波峰焊锡炉焊接的零件。

样　品：每批次抽测 10pcs 样品测试；样品测试前，先对零件的外观作观察，电气参数测试，并记录原始状况。

测　试：1）将样品的引脚距本体 1.5~2.0mm 以下部分浸入锡温为 270+2/-0℃的锡炉中，维持 10±0.5 秒；

2）将样品本体的顶部水平置于锡温为 270+2/-0℃的焊锡表面上方 3~5mm 处，维持 20±0.5 秒；

3）每个样品都要按 1）、2）条方法各进行一次测试判定。

判　定：1）机械特性：测试过的样品，表面用 40 倍以上的放大镜观察零件的包封、引脚接合处，不得有出现破裂现象；引脚强度符合规格书定义要求；零件的塑胶部分不得发生破裂、变形、变色、变脆等现象；PCB 及其它零件的油漆部分不得发生变色、脱落、烧焦等现象。

2）电气特性：测试过的样品，电气参数变化符合规格书定义；

3）记录测试状况，判定结果。

2．回流焊接零件耐焊接热标准

适用范围：所有通过回流焊炉焊接的零件。

样　品：每批次抽测 10pcs 样品测试；样品测试前，先对零件的外观作观察，并记录原始状况。

预　热：将样品置于锡温为 220℃的焊锡表面上方 3~5mm 处，预热 90~120 秒。

测　试：样品预热后，将零件引脚或本体置于锡温为 265+5/-0℃的锡炉中，维持 10+5/-0 秒，样品取出后放置于室温环境中冷却 2 个小时；同一个样品重复预热、测试、冷却过程为一个周期，共进行 3 个周期。

注：ⅰ）贴片电感、贴片电阻、贴片陶瓷电容等电极与本体贴在一起的零件，测试时将整个零件本体都置于锡炉中进行电极的可焊性测试，但贴片的电解电容除外；

ⅱ）贴片变压器、本体较大的贴片零件以及端子或引脚较长者，测试时将零件引脚置于锡炉中进行引脚的可焊性测试。

判　定：1）机械特性：测试过的样品，表面用 40 倍以上的放大镜观察零件的包封、引脚接合处，不得出现破裂现象；引脚强度符合规格书定义要求；零件的塑胶部分不得发生破裂、变形、变色、变脆等现象；PCB 及其它零件的油漆部分不得发生变色、脱落、烧焦等现象。

2）电气特性：测试过的样品，电气参数变化符合规格书定义要求；

3）记录测试状况，判定结果。

AOC EYES VALUE 研发处

Top Victory Electronics(Fujian) Co.,Ltd. Shangzheng Yuanhong Road,Fuqing,Fujian, China Tel: (0591)5285555 5285446 Fax: (0591)5285447
冠捷电子(福建)有限公司 福建省福清市元洪路上郑 E-mail: xiejg@tpv.com.cn web site:http://www.tpv.com.cn

RoHS 零件可焊性试验标准

版本：A　　发布时间：May-18-04　　编写：May-17-04　　核准：May.17.04

1. 波峰焊接零件可焊性标准：

适用范围：所有通过波峰焊锡炉焊接的零件。

样　　品：每批次抽测 5pcs 样品测试；样品测试前，先对零件的外观作观察，并记录原始状况。

预 处 理：将样品的引脚浸入助焊剂（推荐使用优诺-6810 型号）中维持 10±1 秒，浸入焊锡的引脚长度为距本体 1.5~2.0mm 以下部分。

测　　试：将样品引脚距本体 1.5~2.0mm 以下部分浸入锡温为 255 -5/+0℃的锡炉中，维持 2.5±0.5 秒后取出。

判　　定：引脚焊锡面均匀、光滑、沾锡面积≥90%，记录测试状况，判定结果。

2. 回流焊接零件可焊性标准：

适用范围：所有通过回流焊炉焊接的零件。

样　　品：每批次抽测 5pcs 样品测试；样品测试前，先对零件的外观作观察，并记录原始状况。

预 处 理：将样品的引脚浸入助焊剂(推荐使用优诺-6810 型号)中维持 10±1 秒。

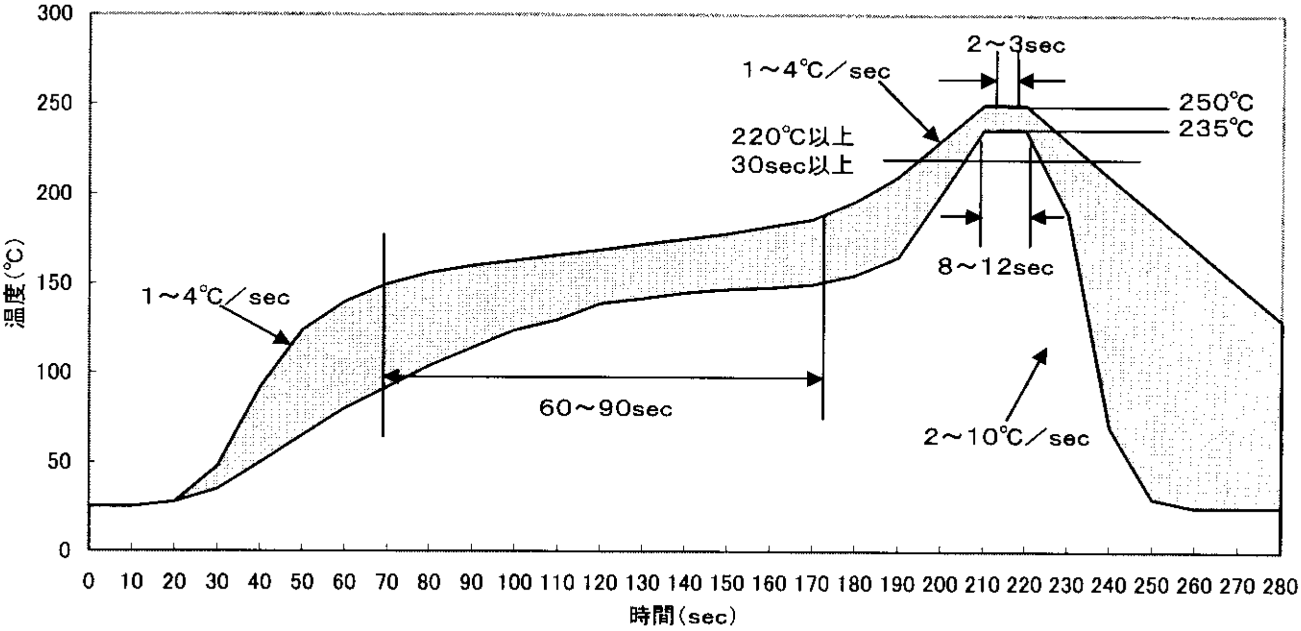
测　　试：将样品引脚浸入锡温为 255-5/+0℃的锡炉中，维持 2.5±0.5 秒后取出。

判　　定：引脚焊锡面均匀、光滑、沾锡面积≥90% ，记录测试状况，判定结果。

3. 1）可焊性测试用的焊锡成分：96.5%Sn+3.0%Ag+0.5%Cu；焊锡的物理特性如附件 item 三；

2）波峰焊、回流焊的工艺参数如附件 item 一、二。

NP303-GM855-GK / NP303-GM855-GQ 推荐温度曲线



一、无铅回流焊制程温度：

1、常温至 150℃的升温速率为 1-4℃/sec；

2、回流时预热温度 150-180℃,约 60-90 秒；

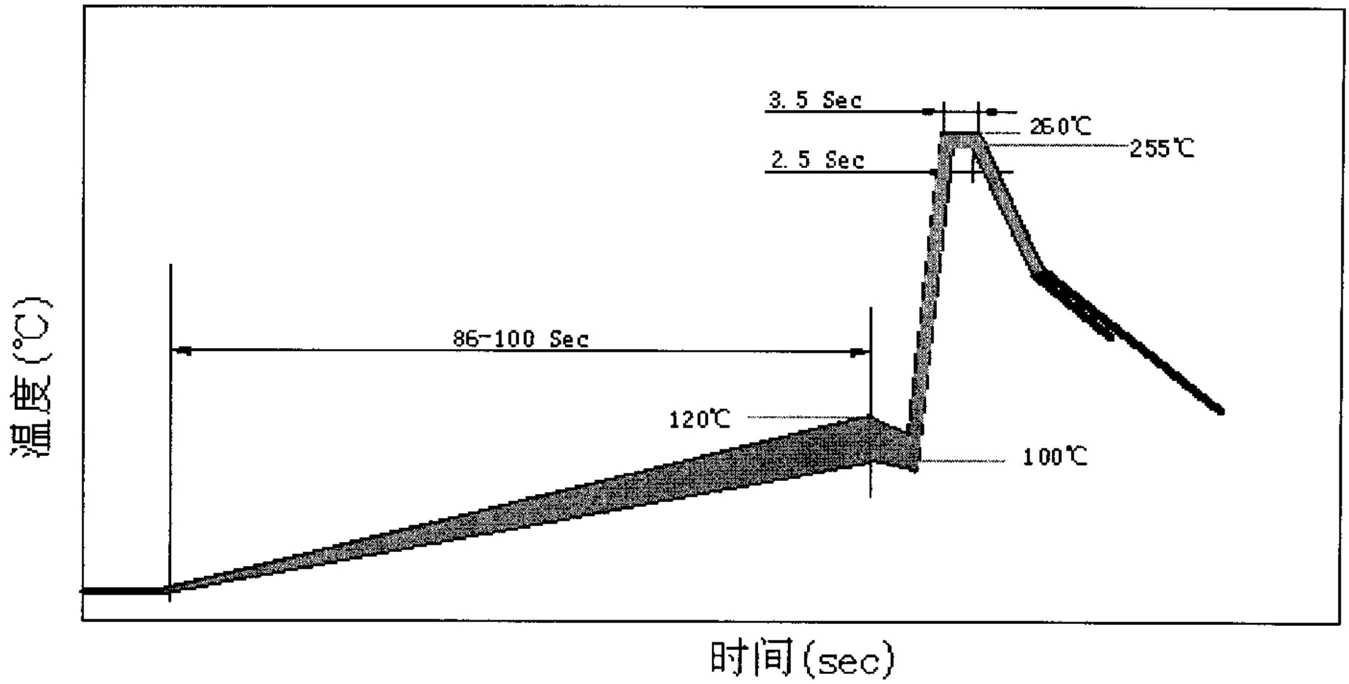
3、220℃以上锡膏加热融化，峰值温度为 235-250℃，总时间 30sec，峰值温度持续时间在 235℃时为 8-12sec，在 250℃时为 2-3sec；

4、降温速率为 2-10℃/sec，从峰值温度降至 183℃时间约 15sec；

5、回流焊总时间约 6Min

为保证零件过回焊炉时能够承受热冲击，零件之耐温规格必须高于锡膏之温度曲线最大温度，即 250℃以上。

无铅波峰焊曲线图



二、无铅波峰焊制程温度：

1、 预热温度 100-120℃，时间 86-100 秒，升温速率为 1-2℃/sec;

2、 零件从预热后即进入 255-260℃的熔锡中；浸入时间为 2.5-3.5sec;

3、 零件焊接后的降温速率为 1-3℃/sec

4、 焊接总时间为 3.5min

为保证零件过波峰焊接时能够承受热冲击，零件之耐温规格必须高于波峰焊接之温度曲线最大温度，即 260℃以上。

三、焊锡参数：

1、焊锡物理成份：

弊司规格	Sn	Pb	Ag	Sb	Cu	Bi	Zn	Fe	Al	As	Cd
96.5Sn3.0Ag0.5Cu	rest	0.1 以下	3.0 ±0.2	0.12 以下	0.5 ±0.05	0.1 以下	0.002 以下	0.02 以下	0.002 以下	0.03 以下	0.002 以下

2、锡棒物理参数：

液相线温度(℃)	221
固相线温度(℃)	216

拉伸强度(kgf/mm^2)	3.7
延展性	33

3、锡膏物理参数：

项目		特性值		试验方法
水溶液抵抗(Ω. m)		1×10^{3}以上		JIS Z 3197 8.1.1 (1999)
助焊剂含有量(wt %)		10.5±0.03		JIS Z 3197 8.1.2(1999)
卤素含量(wt %)		0.07±0.02		JIS Z 3197 8.1.4.2.1(1999)
铜镜腐蚀试验		合格		JIS Z 3197 8.1.4.2.3(1999)
粉末形状及粒度（u m）		GQ	GK	JIS Z 3284 附属书 1
		球形 10-38	球形 20-45	
融点(℃)		216-221		DSC
助焊剂中氟化物试验		不含氟化物		JIS Z 3284 附属书 2
绝缘抵抗 Ω	40℃90%	1×10^{12}以上		JIS Z 3284 附属书 3
	85℃ 85%	5×10^{8}以上		
助焊剂残渣腐蚀性试验		无腐蚀		JIS Z 3284 附属书 4
印刷性		GQ	GK	JIS Z 3284 附属书 5
		0.4mm 间距	0.5mm 间距	
粘度(Pa.s)		180±20		JIS Z 3284 附属书 6
印刷性塌陷性		无 0.2mm 桥连		JIS Z 3284 附属书 7
加热性塌陷性		无 0.2mm 桥桥		JIS Z 3284 附属书 8
粘着性	初期	1．0 N以上		JIS Z 3284 附属书 9
	24 小时后	1．0 N以上		
湿润效力 dewetting		2 级（铜板）		JIS Z 3284 附属书 10
锡球实验	初期	1－3 级		JIS Z 3284 附属书 11
	24 小时后	1－3 级		
回流后残余物粘着性		无粘著性		JIS Z 3284 附属书 12
迁移试验		无发生		JIS Z 3284 附属书 13

GENESIS

To: TPV Electronics (Fujian) Co.,Ltd

Date: 1/12/05

Company: Genesis Micro Chip
Address: 2150 Gold St, Alviso,
CA, 95002

Guarantee of non-use of The Controlled Substances

TPV Electronics (Fujian) Co.,Ltd

We (includes our subsidiary, affiliated company) here guarantee that all the components and parts (includes parts itself and all the packages) shipped to you (includes directly shipping or via third parties) are contained free of those prohibited materials which listed on SONY standard (SS-00259) or its latest version.

1. Cadmium and cadmium compounds
2. Lead and lead compounds
3. Mercury and mercury compounds
4. Hexavalent chromium compounds
5. Polychlorinated biphenyls (PCB)
6. Polychlorinated naphthalenes (PCN)
7. Chlorinated paraffins (CP)
8. Polyvinyl chloride (PVC) and PVC compounds
9. Other chlorinated organic compounds
10. Polybrominated biphenyls (PBB)
11. Polubrominated diphenylethers (PBDE)
12. Other brominated organic compounds
13. Organic tin compounds (Tributyl tin compounds, Triphenyl tin compounds)
14. Asbestos
15. Azo compounds
16. Formaldehyde

Note: In witness where of the above Guarantee has been duly exercised by the company's fully authorized representative signed below.

Signature:
Name: Masood Kafi
Position: Manager

ER1-RD-01 (Ver:01) *Need to affix the official seal, afford by the post or fax.

To: TPV Electronics (Fujian) Co.,Ltd

Date: 12/15/04

Company:Genesis Microchip Inc.
Address: 2150 gold St, Alviso,CA

Guarantee of non-use of The Controlled Substances

TPV Electronics (Fujian) Co.,Ltd

We (includes our subsidiary, affiliated company) here guarantee that all the components and parts (includes parts itself and all the packages) shipped to you (includes directly shipping or via third parties) are contained free of those prohibited materials which listed on SONY standard (SS-00259) or its latest version.

1. Cadmium and cadmium compounds
2. Lead and lead compounds
3. Mercury and mercury compounds
4. Hexavalent chromium compounds
5. Polychlorinated biphenyls (PCB)
6. Polychlorinated naphthalenes (PCN)
7. Chlorinated paraffins (CP)
8. Polyvinyl chloride (PVC) and PVC compounds
9. Other chlorinated organic compounds
10. Polybrominated biphenyls (PBB)
11. Polubrominated diphenylethers (PBDE)
12. Other brominated organic compounds
13. Organic tin compounds (Tributyl tin compounds, Triphenyl tin compounds)
14. Asbestos
15. Azo compounds
16. Formaldehyde

Signature: Masood Kafi
Name: Masood Kafi
Position: Quality Manager

Genesis Microchip Inc

ER1-RD-01 (Ver:01) *Need to affix the official seal, afford by the post or fax.

TO: AOC

DATE:YYYY/MM/DD 2/7/2005

Certificate of non-use of The Controlled Substances

(For Approving, Inspecting and Examining All The Parts)

Suppliers' Trade Code:
Company Name: Genesis Micro Chip
Responsible person's name: Masood Kafi
e-mail: masood. Kafi@gnss.

It is hereby certified that there is neither Sony's required (SS-00259) control level-2(subjected to inhibiting the use) substance nor such use, for such goods having been delivered to Sony as parts and sub-materials, for materials to be used for unit parts, for packing/packaging materials

And, the parts and sub-materials, the materials to be used for unit parts, the packing/packaging materials are all composed of the following components.

（1） Parts, sub-materials and unit parts

Component Name:
Component Part Number: gm2621-LF-AA
SB Part Number:
GB Name:

<Used Material>

No.	Used Position	Material Manufacturer Name	Names of material and Type	GB Part Number
1	Nickel, lead frame composition but not in direct contact with skin			
2	Silver, Die attach epoxy filler content			
3	Tin, solder plating composition			
4				
5				
6				
7				
8				
9				
10				
11				
12				

*＊ If space is insufficient for describing everything, please use the additional sheets

（2） The object of ICP test material(Cd and Pb of Plastic (include rubber), paint, ink and wire)
The request of ICP test data are as given in attached sheets
The composition tables and MSDS of ICP test are as given in attachmented sheets

（3） The immeasurable substance are as given attached sheets
The composition tables and MSDS are as given in attachmented sheets

TPV for SONY Green Partner **RAW MATERIALS & RAW MATERIALS PRODUCER QUESTIONAIRE**

4 Materials TYPE：INKS，PLASTIC，PAINT，WIRE
Approved：IN NOW SONY G/P
是否SONY GP：Process：NEED TO APPROVE BY SONY
X: No need

TPV P/N	TPV SUPPLIER（TPV供应商）	IS SONY GP?	ITEM(品名)	RAW MATERIAL（原材料）	4 Materials TYPE	RAW MATERIAL SUPPLIER原材料供应商	RAW MATERIAL TYPE 原材料型号	IS SONY GP?	Q'ty/Month	Contact	Address（地址）	Mobile No.	Tel.No.	Fax No.	E-mail
	Genesis	[redacted]	Scaler IC	Leadframe	X	[redacted]		X							
				epoxy	Plastic	Sumitomo 1076DS	1076DS	Yes							
				Solder plating	X	[redacted]		X							

Check/Position：Customer Quality Manager

Manager/Position：Masood Kafi

Company: Genesis Micro-Chip

Official seal: ____________